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MIPP Trigger Module

(Conceptual description)

Introduction

The MIPP Trigger Module is designed for generating and distributing through MIPP DAQ system timing synchronization and trigger signals. The requirements for the MIPP trigger system are described in the MIPP internal document [1]. The MIPP DAQ system is built using a unified MIPP Readout Controller Module. The Readout Controller Module distributes timing synchronization and trigger signals in a form of encoded signals synchronous to the distributed 53 MHz clock. The description of the encoding scheme and implemented signals can be found elsewhere [2].

Block-Diagram

The MIPP Trigger Module receives several accelerator related signals:

- Accelerator RF (53.10 MHz nominal value at beam extraction)
- Four decoded beam synchronization signals (BSCLK events)
  - $75 - 120 GeV proton extraction from MI to SWYD
  - $AA - RF/7, zero azimuth marker, occurs on every turn
  - TBD
  - TBD

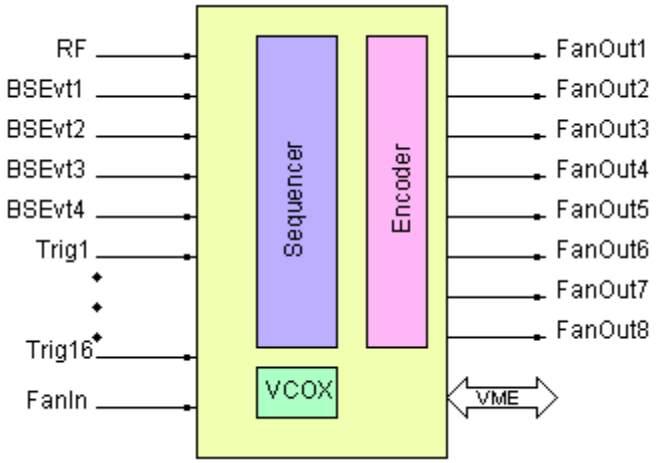


Fig. 1 MIPP Trigger Module

The MIPP Trigger Module generates a sequence of timing control signals encoded into the accelerator RF. The two main signals are Begin Spill and End Spill, which indicate the beginning and the end of the active beam cycle respectively. Asynchronous to the beam INIT, CSTAT and TEST signals are also encoded and can be generated by the module. Logic level Global Reset and Read Event signals are distributed directly via RJ-

45 connector. These signals are to be encoded by the Readout Controller Module and distributed to the front-ends along with the other clock-embedded timing signals. The Readout Controller Module may also generate these two signals independently. The Trigger Module has an internal quartz oscillator, which could be either locked to the accelerator RF or set to a free running mode. The timing sequencer generating beam related signals could be synchronized to the BSCLK events (e.g. $75) or set to run free with a programmable repetition rate.

The module also receives and encodes 16-NIM/TTL input signals as experiment triggers. The definition of various triggers is provided in reference [1]. The encoded trigger signals should be generated only between Begin Spill and End Spill signals.

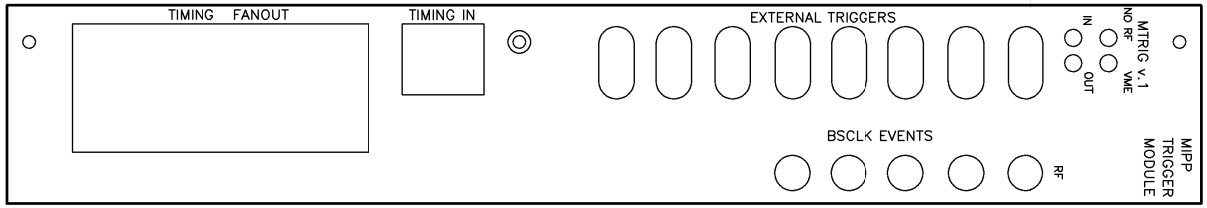
The MIPP Trigger Module has one RJ-45 input and eight RJ-45 output modular connectors. It can be used as a fanout module do distribute timing and control signals within MIPP DAQ crates. The module has a VME slave interface and implemented as a double width 6U VME board. The four signals on RJ-45 connectors have LVDS levels and are listed in the Table 1.

Table 1 RJ-45 connector pinouts

No.	Signal Name	Pin	Comment
1	RFCL+	1	Clear RF, LVDS
2	RFCL-	2	Clear RF, LVDS
3	GRST+	4	Global Reset, LVDS
4	GRST-	5	Global Reset, LVDS
5	RDEV+	3	Read Event, LVDS
6	RDEV-	6	Read Event, LVDS
7	RFTM +	7	Encoded RF, LVDS
8	RFTM -	8	Encoded RF, LVDS

References

[1] Holger Meyer, “Specifications for MIPP readout electronics back end communication,” MIPP-doc-186, April 2007, Unpublished
[2] B.Baldin, S.Hansen, “MIPP Data Cable Protocol,” MIPP-doc-764, April 2008, Unpublished


TIMING FANOUT
TIMING IN
EXTERNAL TRIGGERS
BSCLK EVENTS
RF
IN
OUT
NO RF
VME
MTRIG v.1
MIPP
TRIGGER
MODULE