

MIPP Plastic Ball Electronics Status

Boris Baldin

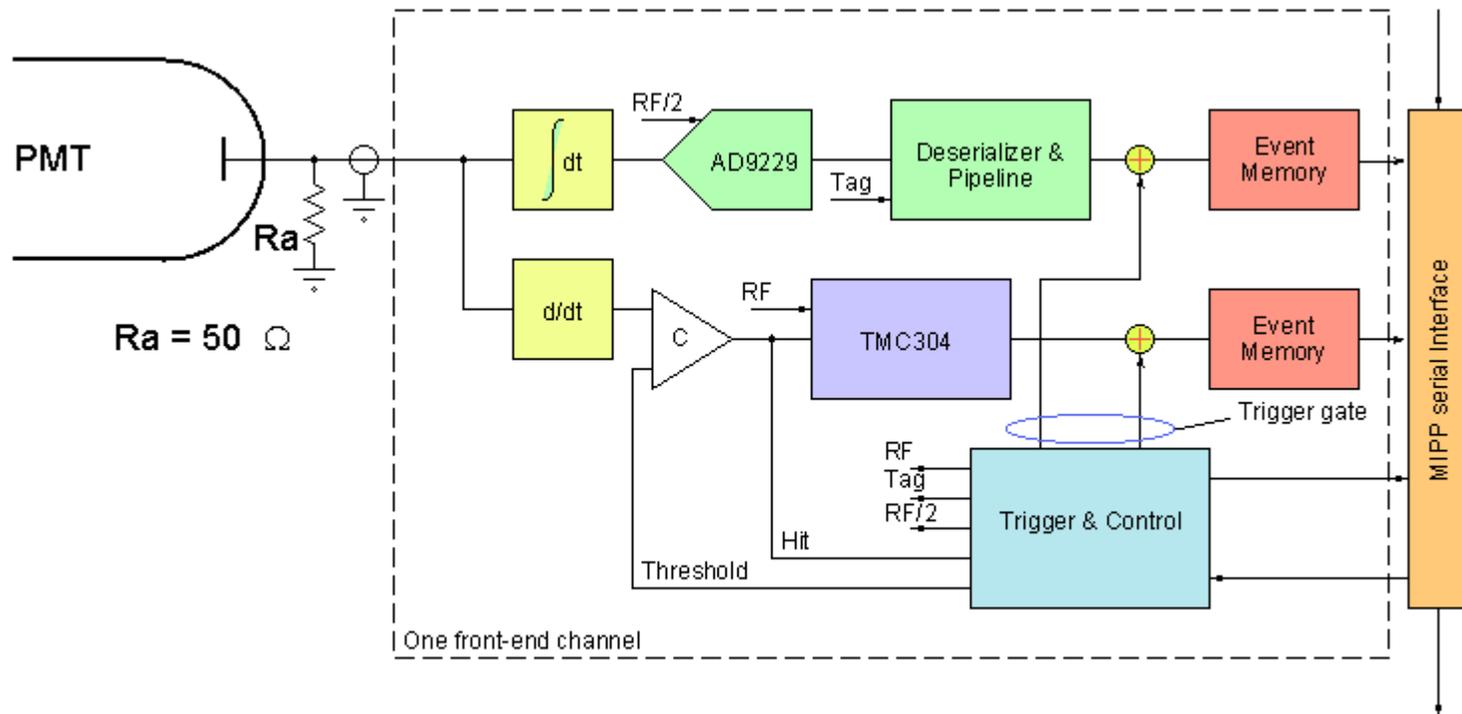
Fermilab

March 07, 2008

General Information

- Total number of channels - 320
- Two component (fast & slow) PMT signal:
 - 10 ns rise/fall time for the fast component
 - 1000 ns fall time for slow component
 - 0.25...1000 pc signal dynamic range
- Trigger decision time - 2 μ s
- Minimum interval between triggers - 16 μ s
- 20,000 events per spill memory storage

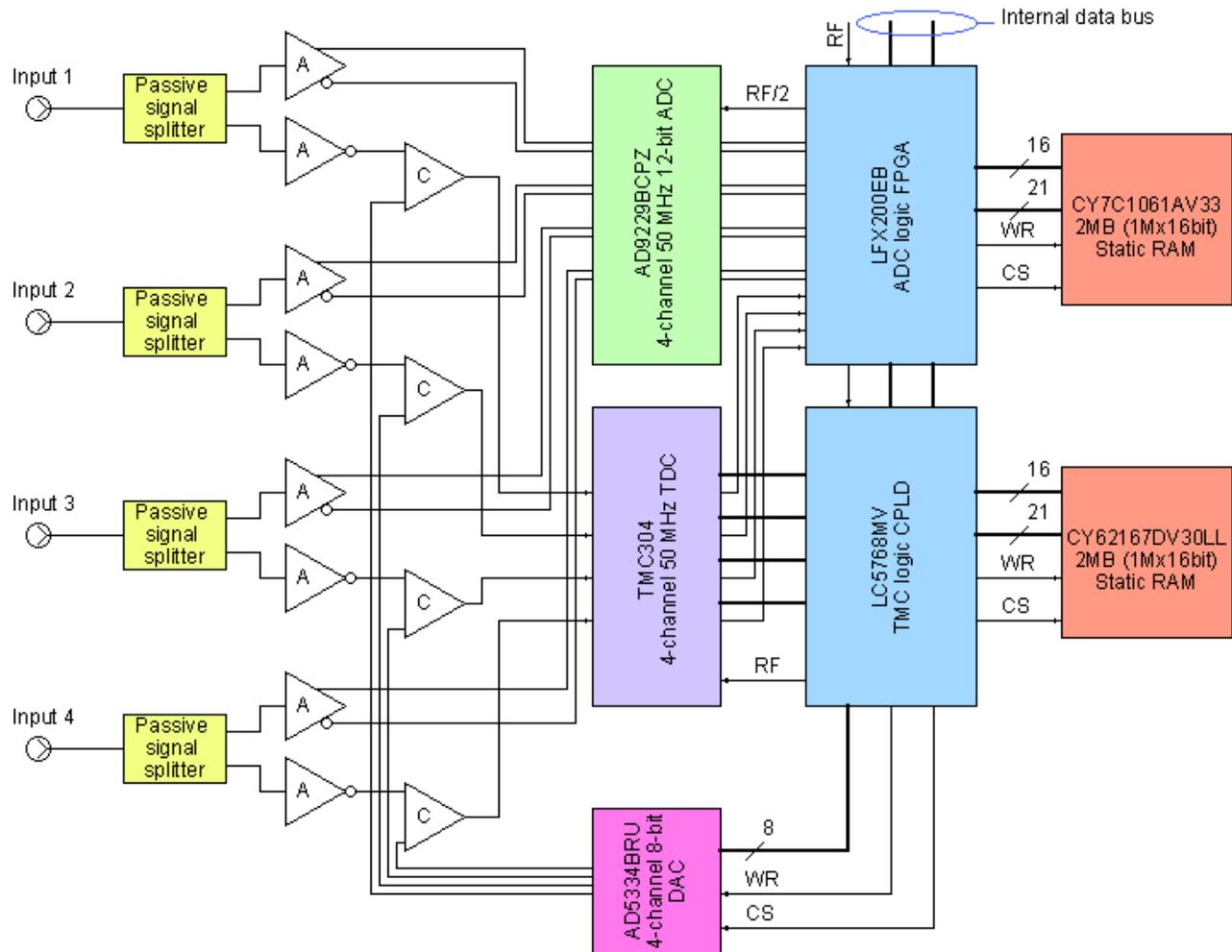
Block Diagram



Design Options

- 8-channel 6U x 220 mm board
- AD9229BCPZ Quad 12-bit pipelined ADC running at $RF/2$ sampling frequency (26.54 MHz)
- TMC304 4-channel Time Digitizer running at RF (53.1 MHz) clock frequency (~ 600 ps time bin)
- Passive signal splitter with integration and differentiation times $\tau_{rc} \sim 20$ ns
- Cypress 2MByte memories to store events from each of four ADC/TDC channels
- Zero suppression using discriminator signal

Detailed Block Diagram



Signal Splitter Simulations



Page 1

SPICE simulation of the passive signal splitter with $\tau = 20$ ns for integration and differentiation and 5 meters of RG-174 cable is shown

Signal rise time is 10 ns, fall times are 10 ns and 500 ns

More detailed information on the PMT signal is needed to adjust splitter parameters

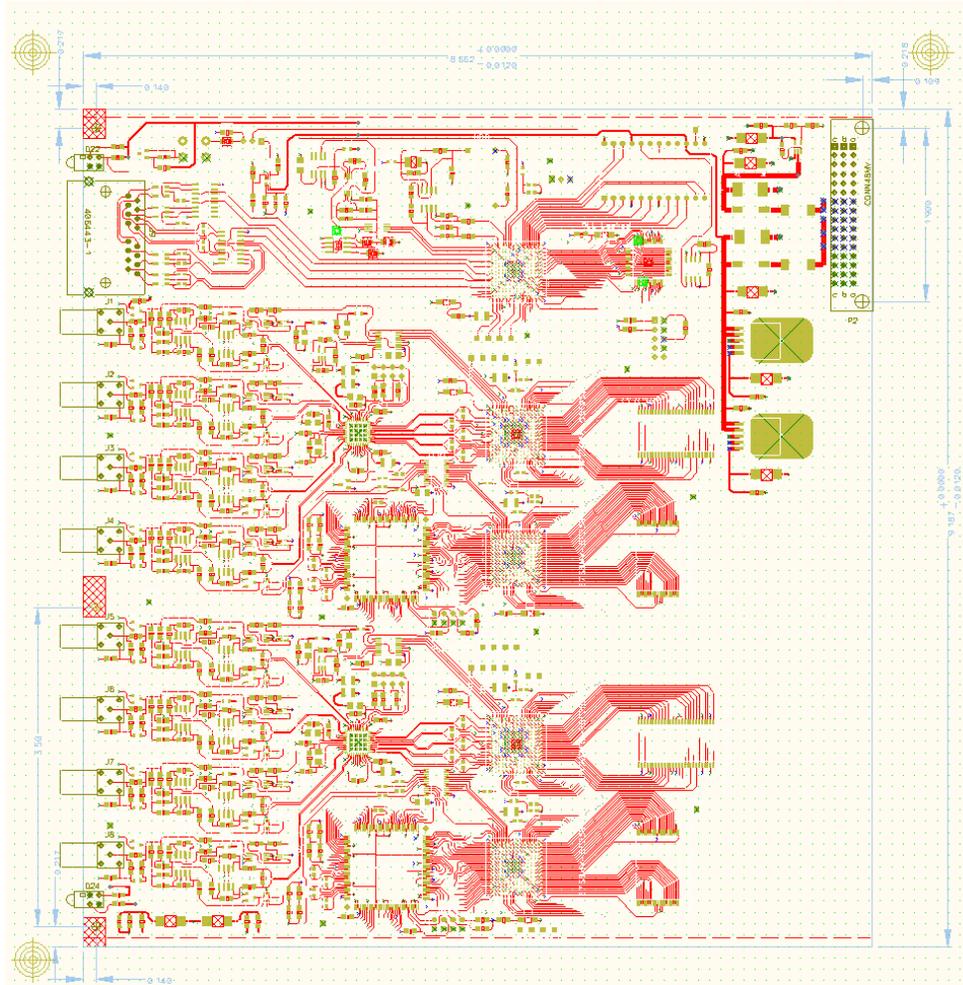
Main design features (1)

- 50-ohm terminated coaxial inputs with isolated ground
- Individual programmable test signal for each channel with 12-bit DAC
- Individual programmable threshold for each channel with 8-bit DAC (8 mV res.)
- Maximum pipeline delay for the TMC304 is 2.4 μ S

Main design features (2)

- Both rising and falling edge TMC time measurements are recorded
- DPM based ADC pipeline delay ($< 9.6 \mu\text{S}$)
- Programmable ADC tag re-triggerable one-shot (5-bit @ 26.55 MHz, $< 1.17 \mu\text{S}$)
- Programmable trigger gate and trigger delay (7-bit @ 53.1 MHz, $< 2.4 \mu\text{S}$)
- On-board temperature measurement

8-channel Board Layout



6U x 220 mm standard
VME size board

Custom 48-pin
backplane connector

All PMT signals and
Readout Interface
cables come to the
front panel

Custom europack (VME) crate



- Based on standard 21-slot VME crate mechanical specification
- Custom backplane is for power distribution only
- Two power supplies:
 - ❑ +5V/60A
 - ❑ -5V/10A
- Possible expansion for +12V/-12V additional power supplies
- Can be used for similar MIPP EMCaI Electronics

Backplane Specification

Connector pinouts for MIPP custom backplane connector 48-pin Eurocard C/2:

GND	+5V	-5V	+12V	-12V	Reserved
A13, A14, A15, A16	A9, A10, A11, A12	A7, A8	A5, A6	A3, A4	A1, A2
B13, B14, B15, B16	B9, B10, B11, B12	B7, B8	B5, B6	B3, B4	B1, B2
C13, C14, C15, C16	C9, C10, C11, C12	C7, C8	C5, C6	C3, C4	C1, C2

Backplane layers (4 total):

Split plane +12V/-12V
Split plane -5V/RES
Solid plane +5V
Solid plane GND

Current Status and Plans

- Schematic design of the PBFEE is complete
- Firmware design with two versions of the readout interface is complete
- PCB layout of the PBFEE is complete
- Five PCBs received from the vendor
- All components for five (5) prototypes are on hand
- Testing of the 1st prototype will start within a few weeks