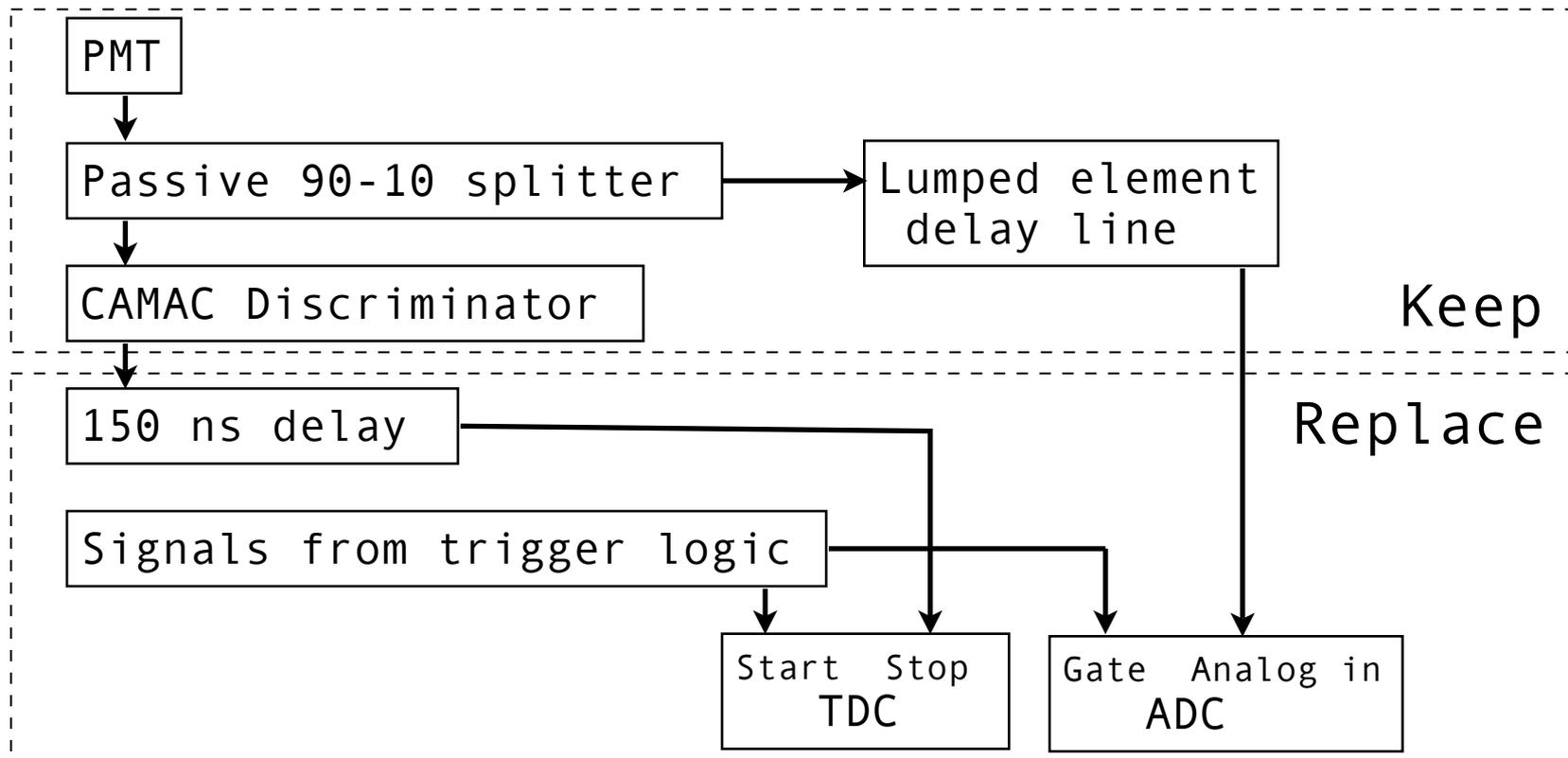


# TOF Electronics for the MIPP Upgrade

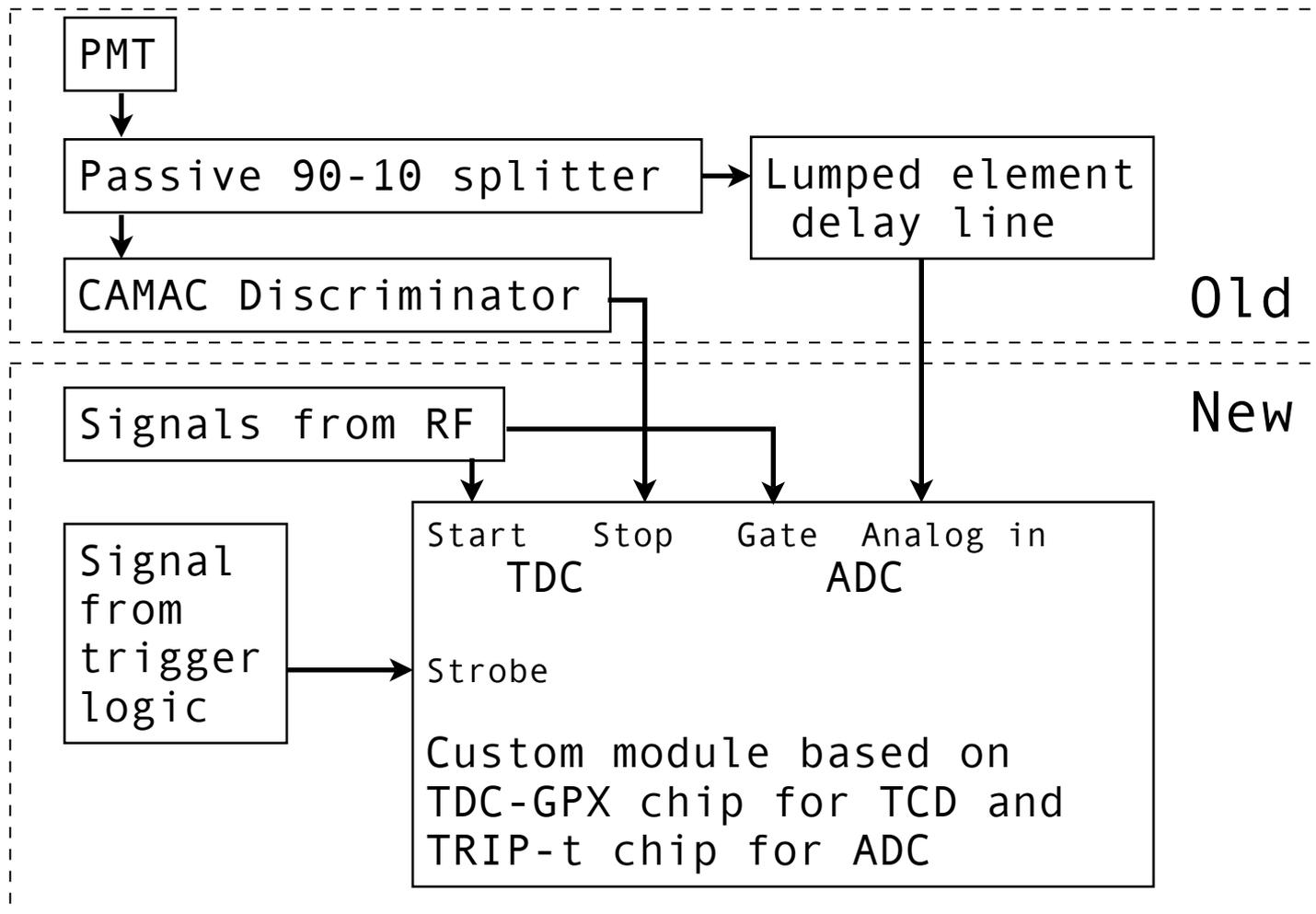
- A very short presentation because exceeding little is known about this system at this time.
- There does not presently exist even a conceptual design.
- All that has been written are statements about what chips will become the basis of a design.

# What we used for MIPP



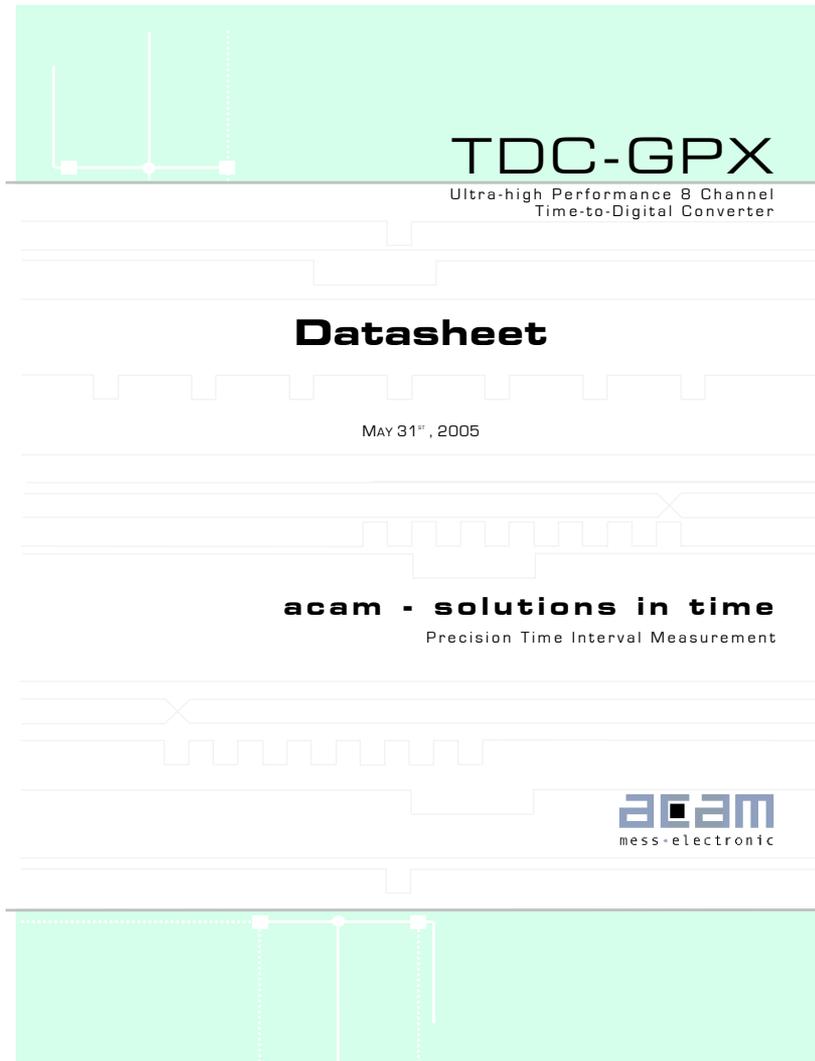
TDC/ADC for T0 and for TOF wall were in different crates at different physical locations.

# What we might use for upgrade



TDC/ADC for T0 and for TOF wall will be in the same crates.

# TDC-GPX Chip



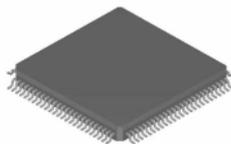
# TDC-GPX Chip



TDC-GPX

## 1. Introduction

### 1.1 System overview



100 TQFP

#### I-Mode

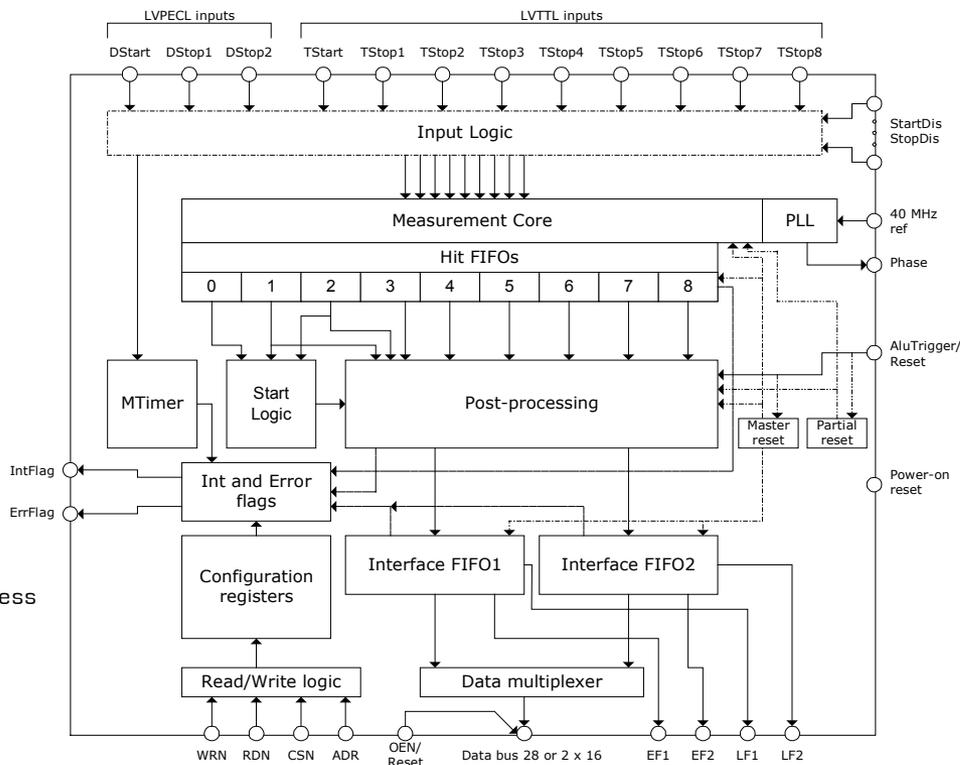
- 8 channels with typ. 81 ps resolution
- LVTTTL inputs, optional LVPECL
- 5.5 ns pulse-pair resolution with 32-fold multi-hit capability = 182 MHz peak rate
- Trigger to rising or falling edge
- Measurement range 9,8  $\mu$ s, endless measurement range by internal retrigger of START
- 10 MHz continuous rate per channel
- 40 MHz continuous rate per chip

#### G-Mode

- 2 channels with 40 ps resolution
- Differential LVPECL inputs, optional LVTTTL
- Measurement range 0 ns to 65  $\mu$ s
- 5.5 ns pulse-pair resolution between edges of equal slope with 32-fold multi-hit = 182 MHz peak rate

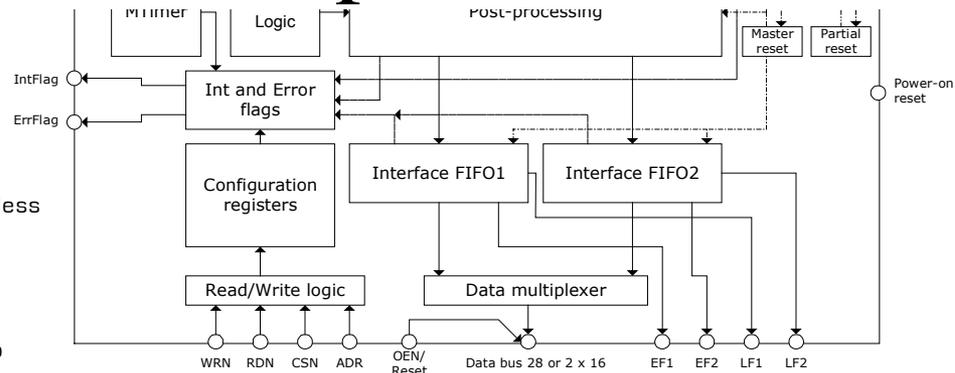
#### M-Mode

- 2 channels with 10 ps resolution [70 ps peak-peak]
- Differential LVPECL inputs
- Measurement range 0 ns up to 10  $\mu$ s
- Single hit per Start and channel



# TDC-GPX Chip

- resolution
- LVTTTL inputs, optional LVTTTL
- 5.5 ns pulse-pair resolution with 32-fold multi-hit capability = 182 MHz peak rate
- Trigger to rising or falling edge
- Measurement range 9,8  $\mu$ s, endless measurement range by internal retrigger of START
- 10 MHz continuous rate per channel
- 40 MHz continuous rate per chip



## G-Mode

- 2 channels with 40 ps resolution
- Differential LVPECL inputs, optional LVTTTL
- Measurement range 0 ns to 65  $\mu$ s
- 5.5 ns pulse-pair resolution between edges of equal slope with 32-fold multi-hit = 182 MHz peak rate
- Minimum pulse width 1.5 ns
- Trigger to rising **and** falling edge
- Optional Quiet Mode [no ALU operation and Data-output during measurements]
- 20 MHz continuous rate per channel
- 40 MHz continuous rate per chip

## R-Mode

- 2 channels with 27 ps resolution
- Differential LVPECL inputs, optional LVTTTL
- Measurement range 0  $\mu$ s up to 40  $\mu$ s
- 5.5 ns pulse-pair resolution with 32-fold multi-hit capability = 182 MHz peak rate
- Trigger to rising or falling edge
- Optional Quiet Mode [no ALU operation and Data-output during measurements]
- 40 MHz continuous rate per channel
- 40 MHz continuous rate per chip

## M-Mode

- 2 channels with 10 ps resolution (70 ps peak-peak)
- Differential LVPECL inputs
- Measurement range 0 ns up to 10  $\mu$ s
- Single hit per Start and channel
- Trigger to rising or falling edge
- Quiet Mode [no ALU operation and Data-output during measurements]
- Max. 500 kHz continuous rate per channel
- Max. 1 MHz continuous rate per chip

## General

- Start retrigger option (besides M-Mode)
- Package: 100 TQFP
- IO voltage 3.0 V - 3.6 V
- Core voltage 2.3 V - 3.6 V regulated by resolution adjust unit
- Data bus: 28 Bit or 2 x 16 Bit asynchronous with Chipselect, Readstrobe, Writestrobe
- 40 MHz continuous rate per chip
- Address range: 4 Bit

# TDC-GPX Chip

## 1.3.4 Reset Timings

(V<sub>ddo</sub> = V<sub>ddc</sub> = 3.3 V, T<sub>a</sub> = +25°C)

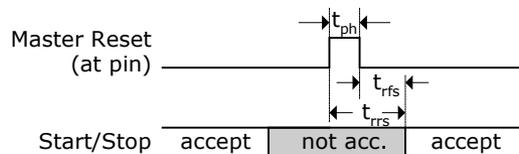


Figure 7

Spec	Description	Min (ns)	Max (ns)
$t_{ph}$	Reset pulse width	10	-
$t_{rfs}$	Time after rising edge of reset pulse before hits are accepted	27	-
$t_{rrs}$	Time after falling edge of reset pulse before hits are accepted	13	-

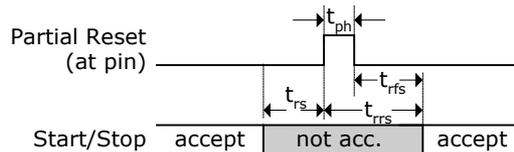


Figure 8

Spec	Description	Min (ns)	Max (ns)
$t_{ph}$	Reset pulse width	10	-
$t_{rfs}$	Time after rising edge of reset pulse before hits are accepted	60	-
$t_{rrs}$	Time after falling edge of reset pulse before hits are accepted	13	-
$t_{rs}$	Time before rising edge of reset pulse where hits will be lost	-	37

# TDC-GPX Chip

- Design issues
  - Reset creates deadtime of  $\sim 100$  ns. At what intervals do we reset and restart? Cannot exceed  $40 \mu\text{s}$ .
  - The chip internally buffers up to 32 hits, but how will it allow us to match “hits” with start pulses / RF buckets? Is it necessary to match hits with RF buckets?
  - The “time constant” of these chips follows a distribution of some width. Do we have to calibrate the chips individually?

# TDC-GPX Chip

- Design issues
  - Almost certainly we need two operating modes, one in which the trigger strobe serves to “sparsify” the output stream and another in which it does not.
  - Possibly good news: Other HEP experiments are planning to use this chip.
  - Not so good news: ~\$200/chip.

# A Suggestion for TDC-GPX Usage

- Introduce a new periodicity into the trigger / DAQ logic: an “MI turn.”
- MI turns have a duration of  $\sim 10 \mu\text{s}$ .
- The experiment is necessarily dead during the “abort batch,”  $\sim 1.5 \mu\text{s}$ . (We can probably afford to depopulate one batch adjacent to the abort batch yielding a “quiet interval” of  $\sim 3.0 \mu\text{s}$ .)
- At end of quiet interval reset and send a start pulse to all TOF modules.
- At beginning of quiet interval determine presence of an event during the turn. If present, move data from volatile memory to intermediate memory (where time stamps get attached.)

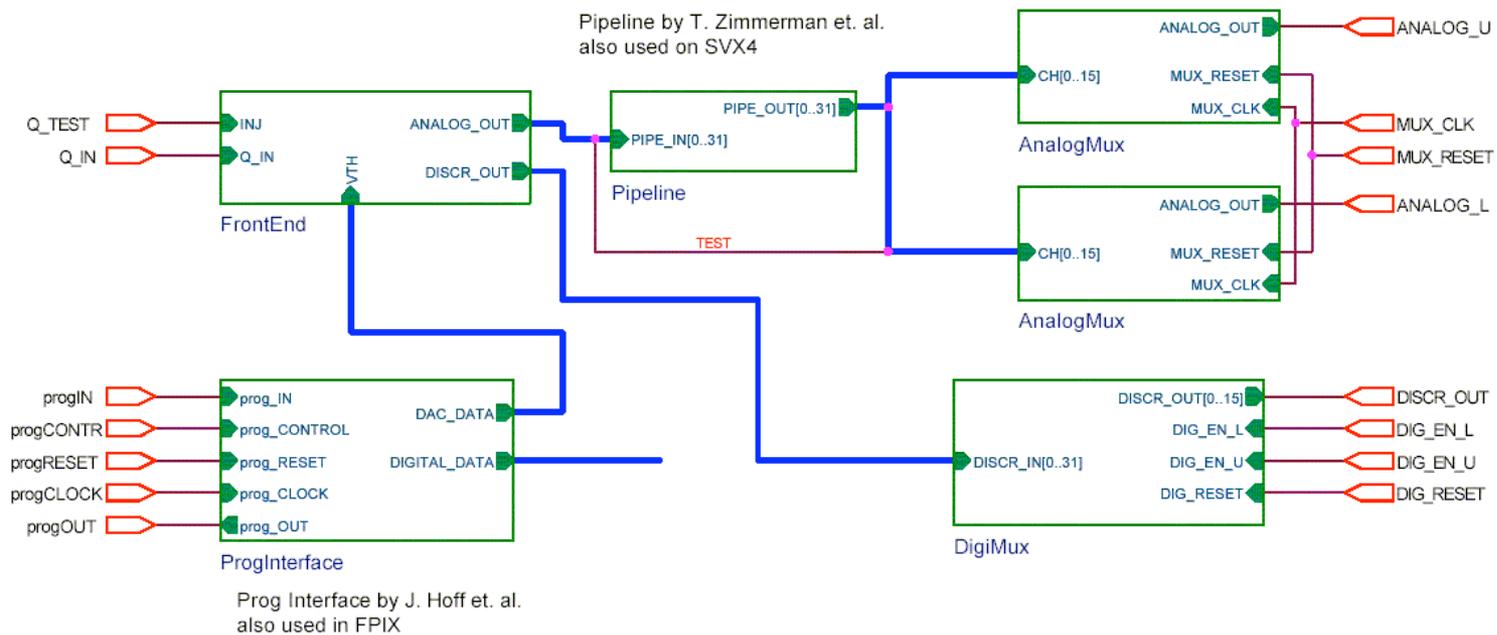
# ADC with TRIP-t Chip



## Trip Chip



### Simplified schematic



# ADC with TRIP-t Chip

## Description of the TRIP-t

The TRIP-t chip, designed by Abderrezak Mekkaoui, Tom Zimmerman and Jim Hoff is the part of the front end of the D0 electronics for the VLPC based detectors. Its inputs are the analog pulses from the fibers after amplification by the VLPCs and digital timing inputs to control e.g. the time window over which the system should be sensitive to pulses. The outputs of the TRIP-t are (1) a digital signal to use for triggering; (2) an analog pulse ( $\sim 1V$ ) that is proportional to the amplitude of the input from the VLPC, called the *A*-pulse; (3) an analog pulse ( $\sim 1V$ ) that is proportional to the time between the firing of the discriminator and the closing of the time-gate, called the *t*-pulse. The chip contains an analog pipeline just before the final output drivers.

The TRIP-t is a modification of the TRIP chip; see D0 notes 4009 and 4076. Documentation is at [smb://D0server6/projects/TriggerElectronics/CAE/Run\\_I Ib\\_AFE](smb://D0server6/projects/TriggerElectronics/CAE/Run_I Ib_AFE).

Figure 1 shows a simplified functional diagram of the TRIP-t. The front end, shown in simplified functional form in Figure 2, produces the three primary outputs of the chip. The *A*-pulse and *t*-pulse outputs are stored in analog pipelines, and the output of these is selected by the SKIPB signal, which is in effect the L1 YES signal. Outputs to form trigger signals are created by discriminators in the front end, and readout quickly through the digital multiplexer. The operation of the front end is controlled by a set of DACs that determine parameters such as the drive currents for opamps. Although it is not shown in Figure 1, the Program Interface also provides some parameters to the pipeline and the final output drivers of the *A*- and *t*-pulses.

## Operation of the TRIP-t

The programming of the DACs for the TRIP-t is basically the same as it was for the TRIP chip, and is described in D0 note 4009. However, the meanings of the registers given in that document have changed. The new definitions and the values used here are given in Table 1. The values used here should be close to those used in the final installation, except for registers 6 and 11.

Correct operation also requires specification of the timing of the signals input to the chip. A spreadsheet showing all the signals is available at [smb://D0server6/projects/TriggerElectronics/CAE/Run\\_I Ib\\_AFE/Trip-t\ Chip/TRIP-t\ from\ Leo/Review\\_Apr05/DG2020\ copy.xls](smb://D0server6/projects/TriggerElectronics/CAE/Run_I Ib_AFE/Trip-t\ Chip/TRIP-t\ from\ Leo/Review_Apr05/DG2020\ copy.xls). Figure 3 shows a detail of the critical reset/gating signals.

The PRE\_RST signal is actually three signals; PRE\_RST itself, and two inverted signals, P2A\_RSTB and P2B\_RSTB. All have the same timing; the reset is on for  $245ns$  and then off for  $155ns$ , making a cycle time of  $400ns$ , close to the  $393ns$  beam crossing time. The signals DIGENL, DIGENU, and DIGENB are the signals to output the discriminator signals; the first 16 channels are sent out on DIGENL and the same 16 lines show the second 16 discriminator results on DIGENU. These signals are  $20ns$  wide and their positioning inside the PRE\_RST pulse is not critical. The PLN\_CLK signal determines the gate for which the input is sensitive, unless PR1 was high at an earlier low to high transition of PLN\_CLK. In the latter case, the pipeline is read out. In figure 3, the chip will be sensitive to pulses at the input between  $t = 9420ns$  and  $t = 9520ns$ . PRE\_RST

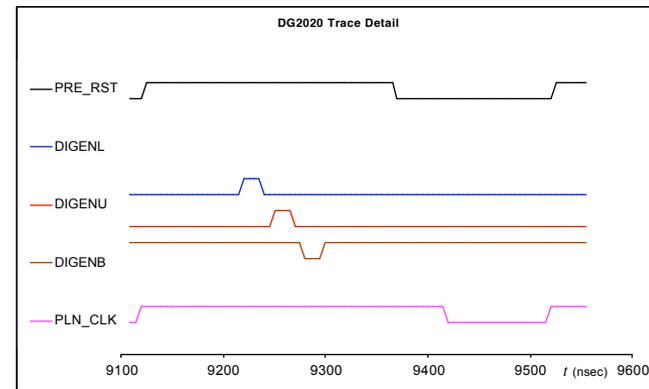


Figure 3. Reset and gating signal details

must finish  $50ns$  before the PLN\_CLK is active, and there is a  $5ns$  gap after the gate closes before the next PRE\_RST begins.

# ADC with TRIP-t Chip

- TRIP-t chip is a Fermilab design. A conventional manufacturer's data sheet is hard to find.
- Hard to decipher from existing documentation, graphic or English, what this chip does and how to use it.
- Nonetheless we can reasonably expect that the TRIP-t chip or some other chip will do for the pulse height what the TDC-GPX chip does for the timing.
- Much *design* work remains to realize a custom TOF module.

# The Road Ahead

- Much *design* work remains to realize a custom TOF module.

*Finis*