

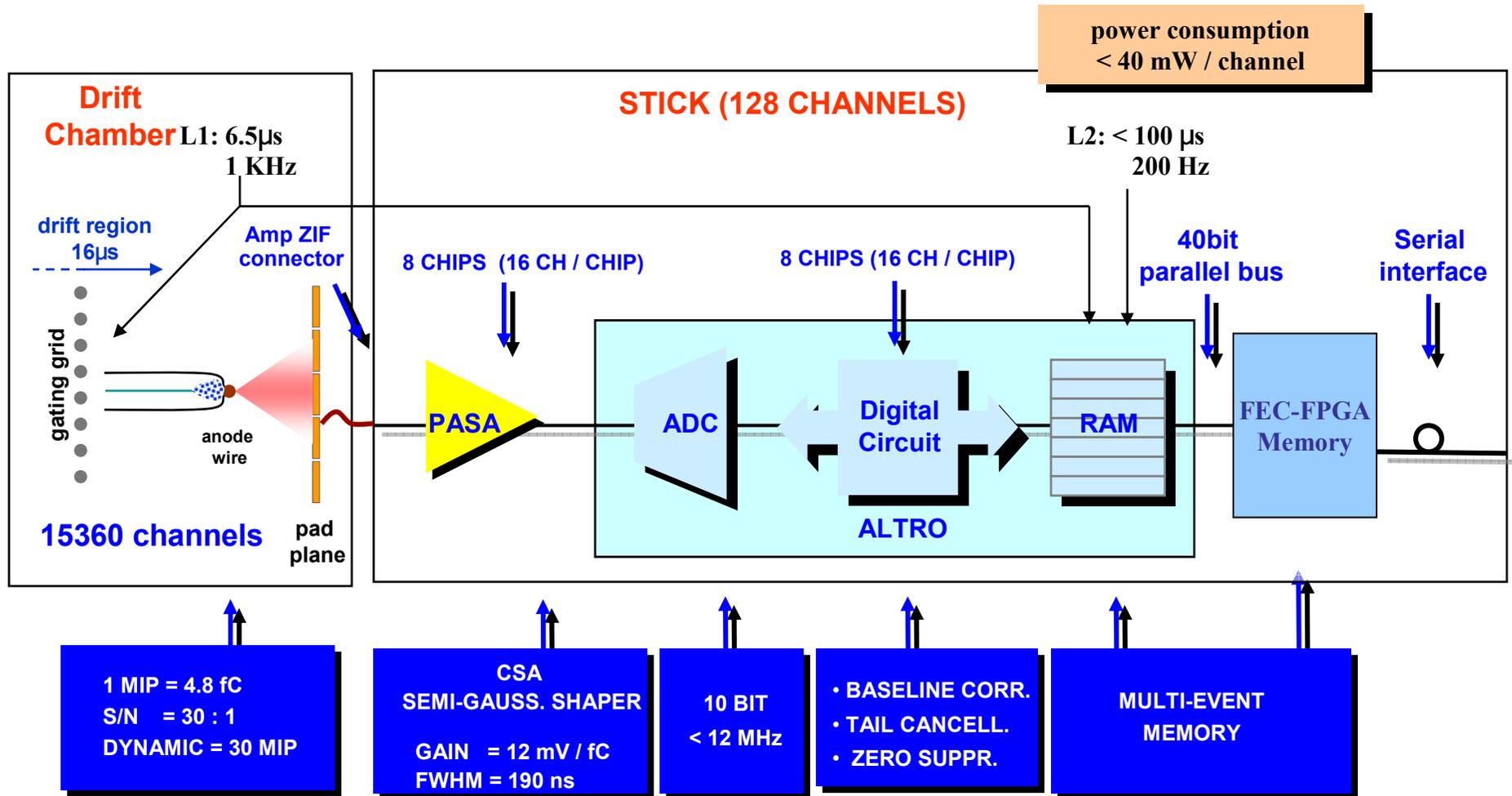
TPC electronics Status, Plans, Needs

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Short list of topics

- The Pasa/Altro chips (have been purchased)
- Mipp TPC data path requirements
- Design and layouts of new Sticks
- Altro chip specifics intro.



Data Path Requirements of TPC

- The SY120 program will switch to one 4 second slow spill every 2 minutes.
- The drift volume height is 75cm, corresponding to a maximum collection time of 15usec.
- The TPC grid is currently limited to a maximum pulse rate of 3kHz.
- The readout should be capable of a sustained rate of .3ms per event and a burst rate of .2ms per event.
- The 15360 channels of TPC are used to measure particle trajectory momentum and dE/dx .
- The detector is currently instrument with 128 analog/digital electronics cards “sticks” which would be designed to have PASA/ALTRO chips. $15360/128=120$
- For the TPC there will be 250 samples per event channel to match the drift time of the detector.
- With a zero suppressed event size estimated to be 115kb for multi track events.

Data Path of TPC

- A 575mb/s burst rate readout could be achieved with 5-way parallel 115mb/s datapaths.
- Each PASA/ALTRO chip sets has a 10bit 40MHz. ADC, with digital signal processor and memory buffer.
- The chips are controlled over a 40bit wide bus that supports 200MB/s.
- The ALTRO event buffer will be able to fully buffer 8 events.

TPC 15360 channels 15us drift time
 3kHz maximum readout (300us)
 115kbytes est. event
 20MHz sample clk

← 4sec. spill every 120sec

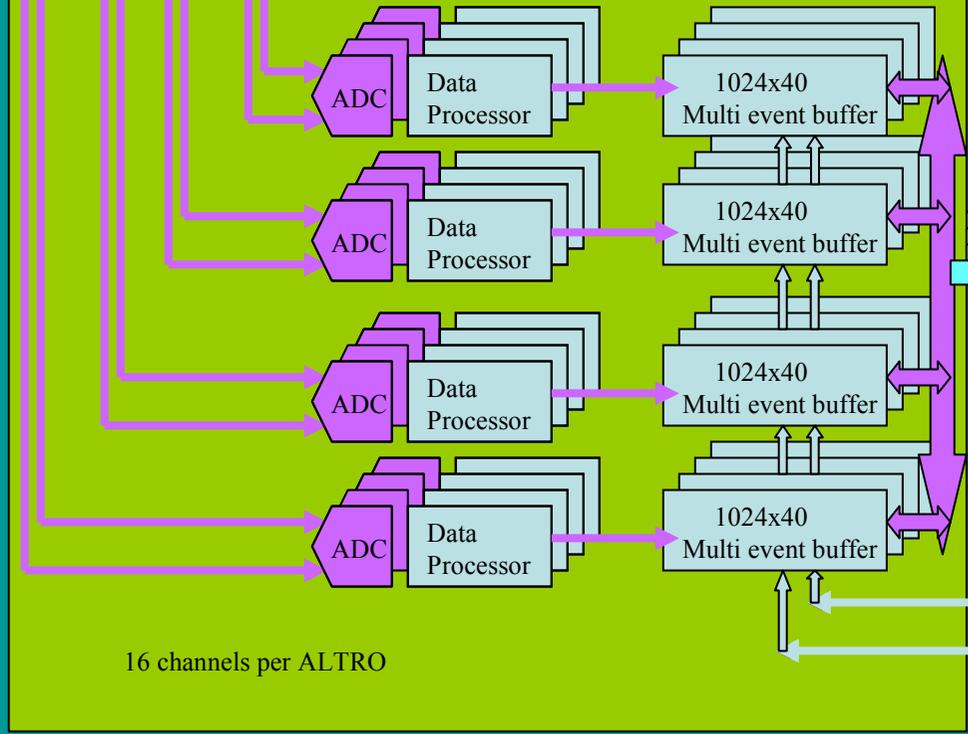
Rate into Readout System

$115\text{kbytes}/300\mu\text{s} = 383\text{Mbytes}/\text{sec}$
 $4\text{sec} \times 383\text{Mbytes}/\text{sec} = 1532\text{Mbytes}/\text{spill}$
 $1532\text{M}/120 = 12.8\text{Mbytes}/\text{sec}$

$250\text{bytes}/\text{event per ch} \times 16\text{ch per Pasa-Altro} = 4000\text{bytes}/\text{event}$
 $1/300\mu\text{s} = .3\text{m max event rate}$
 $4000/.3\text{m} = 13.3\text{Mbytes}/\text{sec. per Pasa-Altro}$
 $8 \times 13.3\text{Mbytes} = 106.4\text{Mbytes}/\text{sec per Stick}$

PASA
 16 channel per PASA
 250 samples per channel per event

10 bit ADC 20MHz **ALTRO**



200Mbytes/sec 40bit data path (40MHz. Rclk)
 Per ALTRO

Front end card buffer controller
 8 ALTRO per Buffer

LV2 Trig
 LV1 Trig

← 20MHz master clock (sample rate)

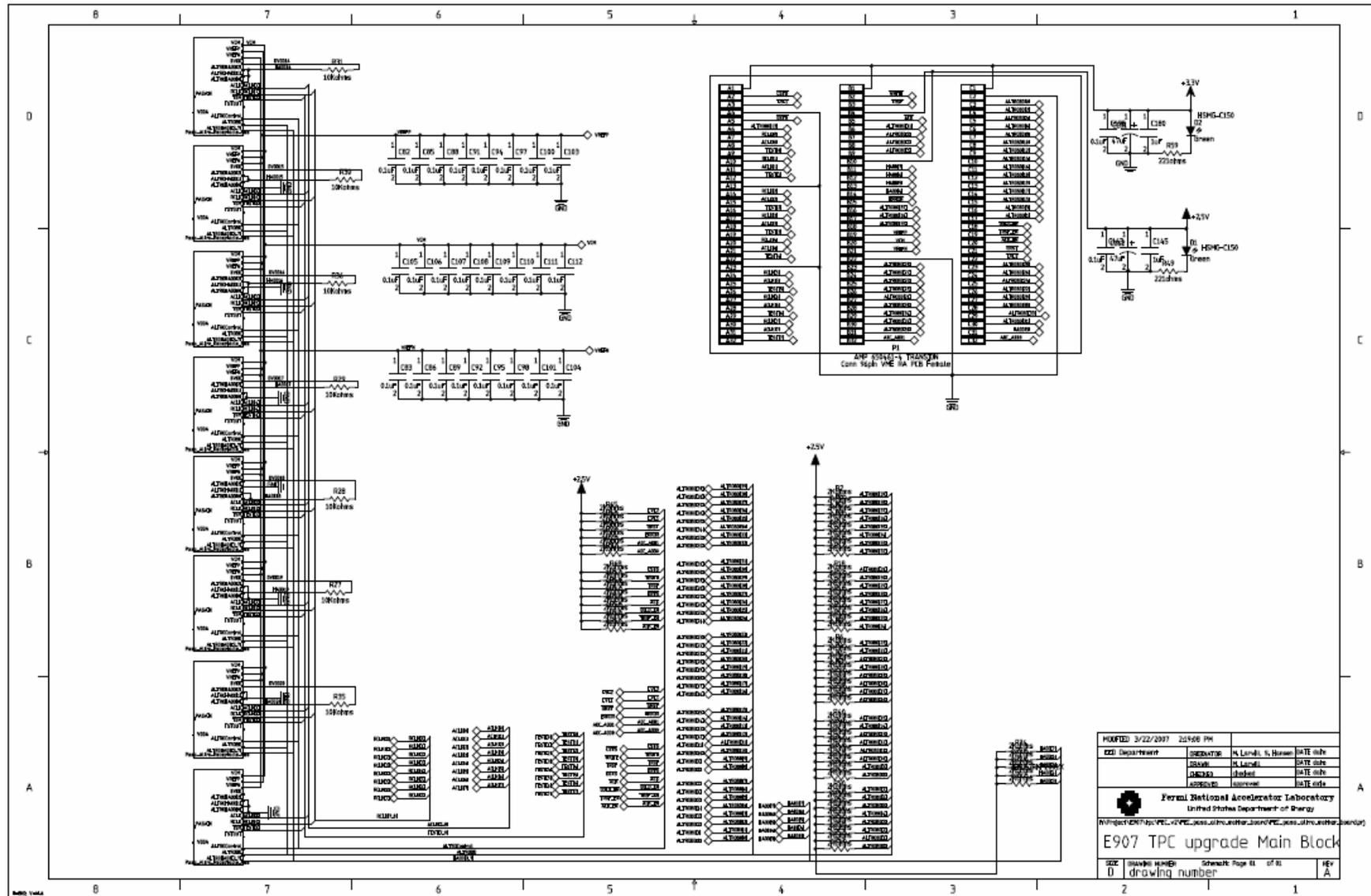
8 Pasa-Altros x 16 ch each stick = 128 ch per stick
 (?)# 124 sticks

How we compare to E907 Front End Cards (Sticks)

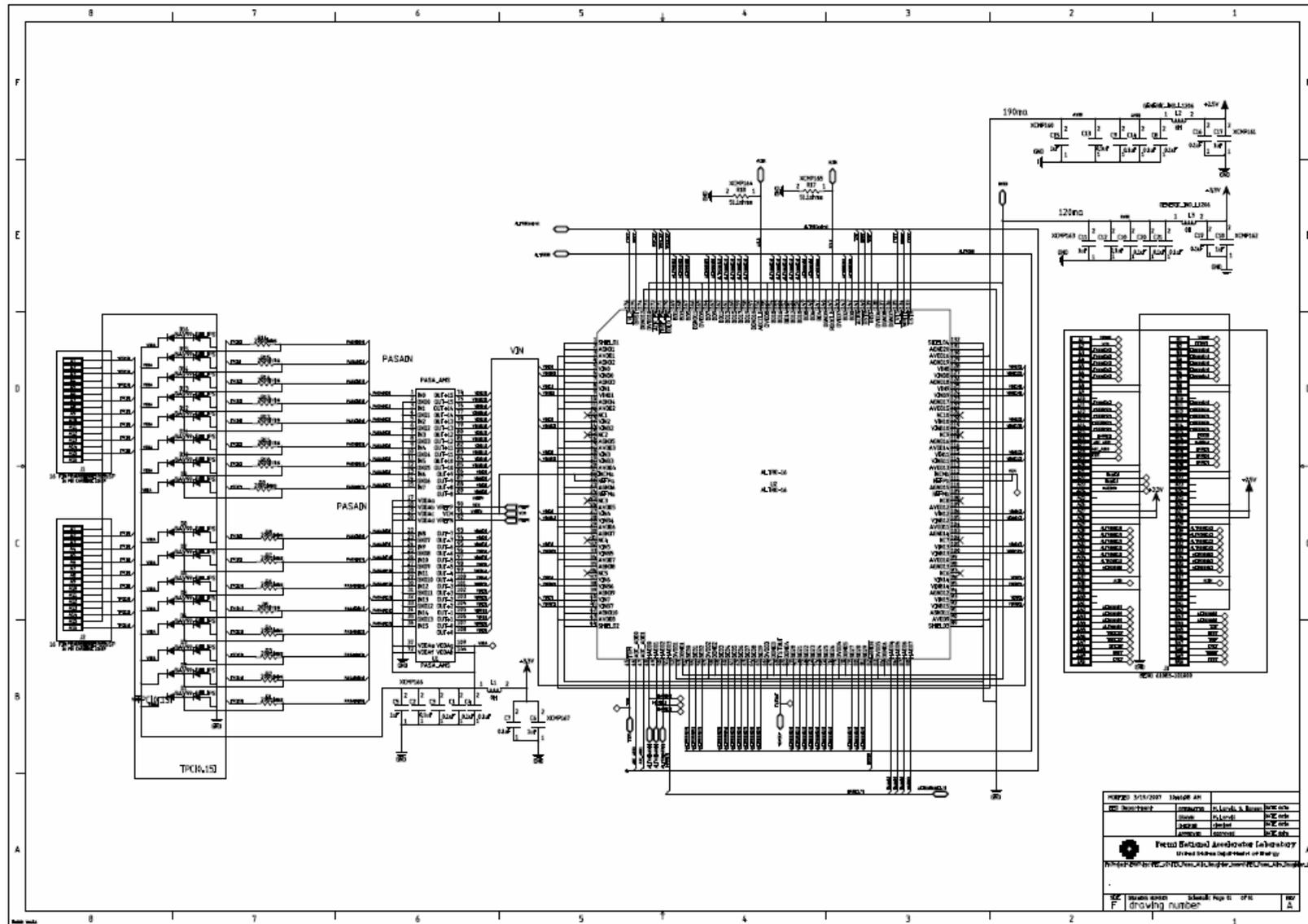
The “sticks,” sit in the electronics bay just below the pad plane. The sticks are multi-layer boards mounted on aluminum for cooling. When installed, the base of the stick assembly is in contact with the bottom of the electronics bay, which is water-cooled.

There are on-board power and interlock connections. The exhaust passes a smoke detector on the AC interlock loop. The sticks connect to the pad plane through a ZIF card edge connector. The pad plane and ZIF connector, encode the stick slot position and form an interlock for proper card insertion. If the card is not completely inserted, the interlock contacts are not made up, and the DC power supply interlock will not make up for that stick, preventing power from being applied to the board. The sticks also contain a thermal limit switch, set to open at 40°C, in the interlock chain.

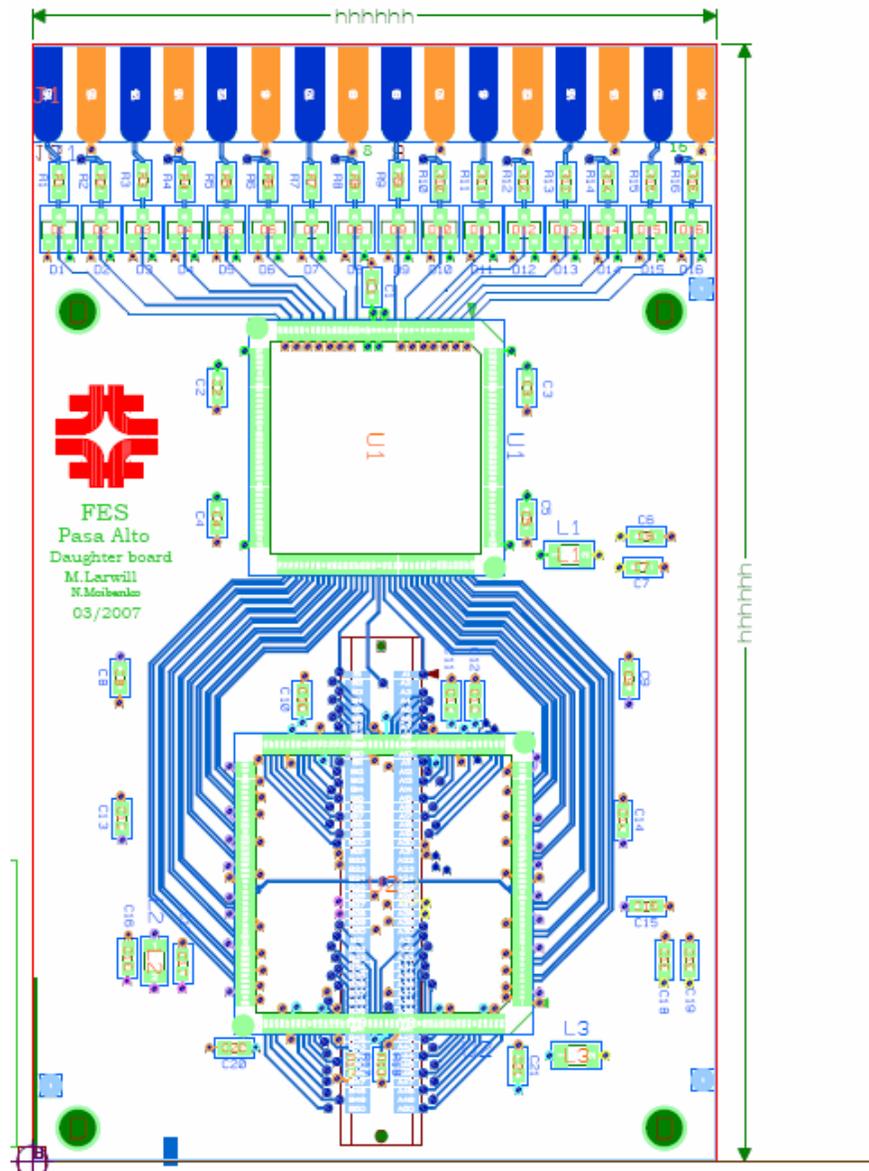
Prototype Top level schematic of Altro/Pasa chips on Stick for Mipp



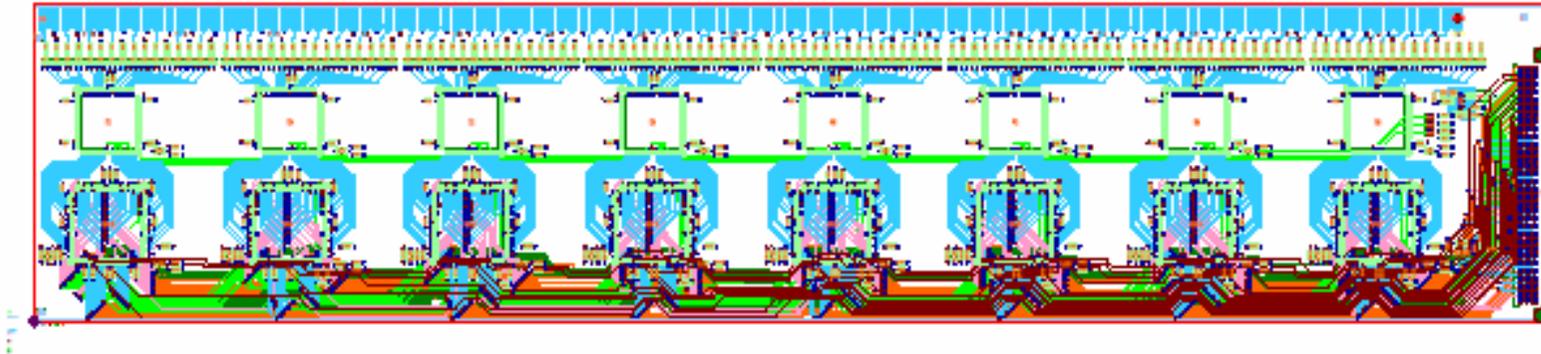
Schematic of Pasa/Altro chip set



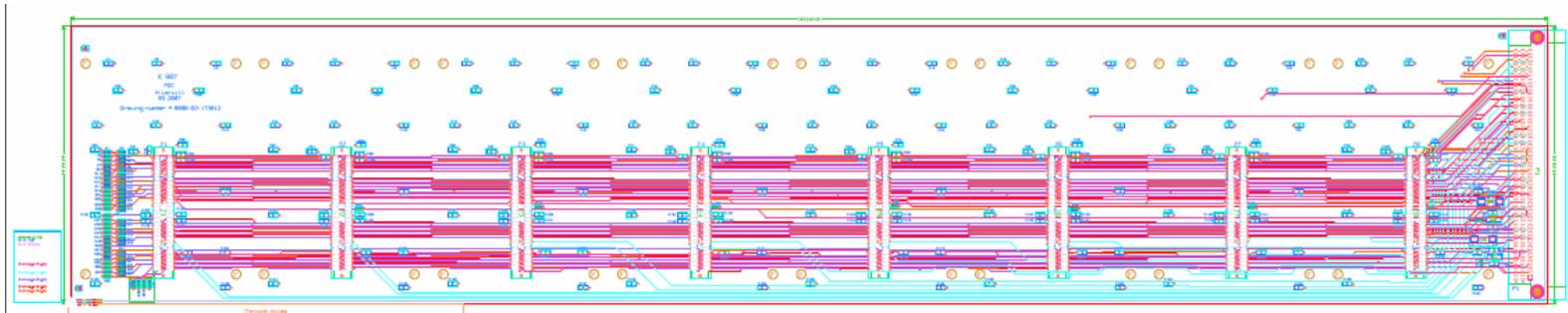
Daughter card layout of Pasa/Altro chip set



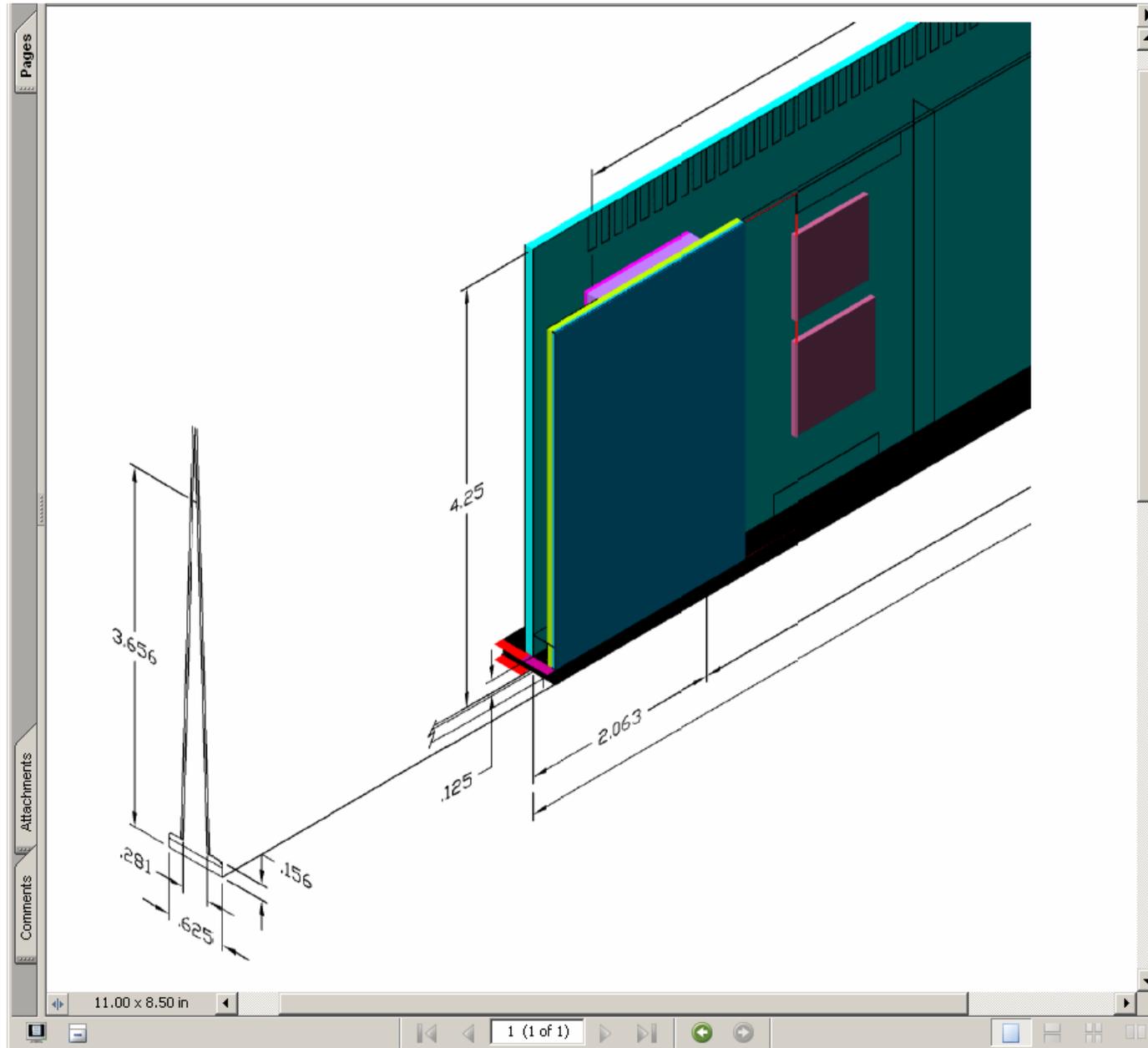
Layout of Stick with Pasa/Altro chip set on main board



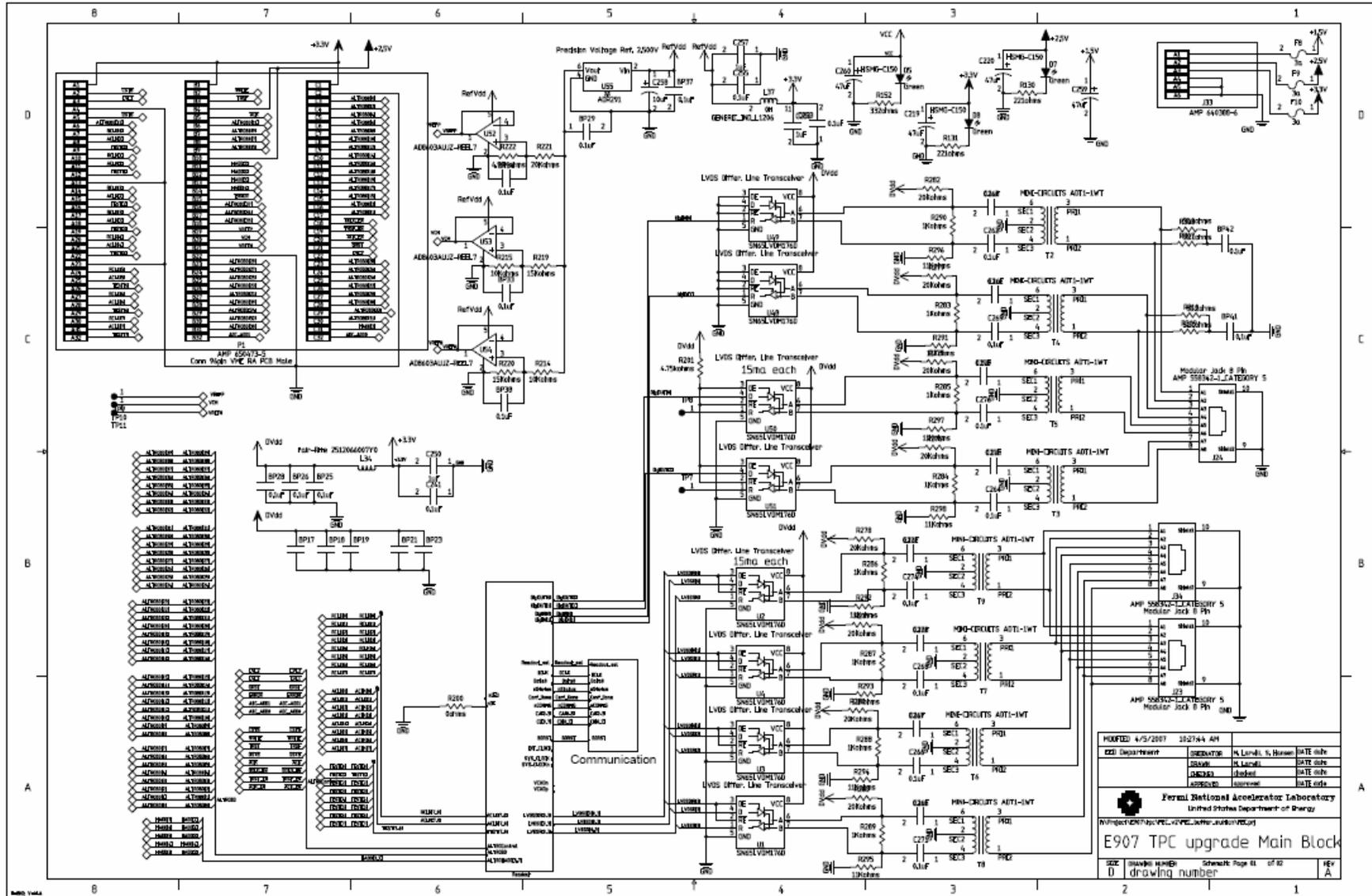
Layout of Stick with Pasa/Altro chip set on daughter cards



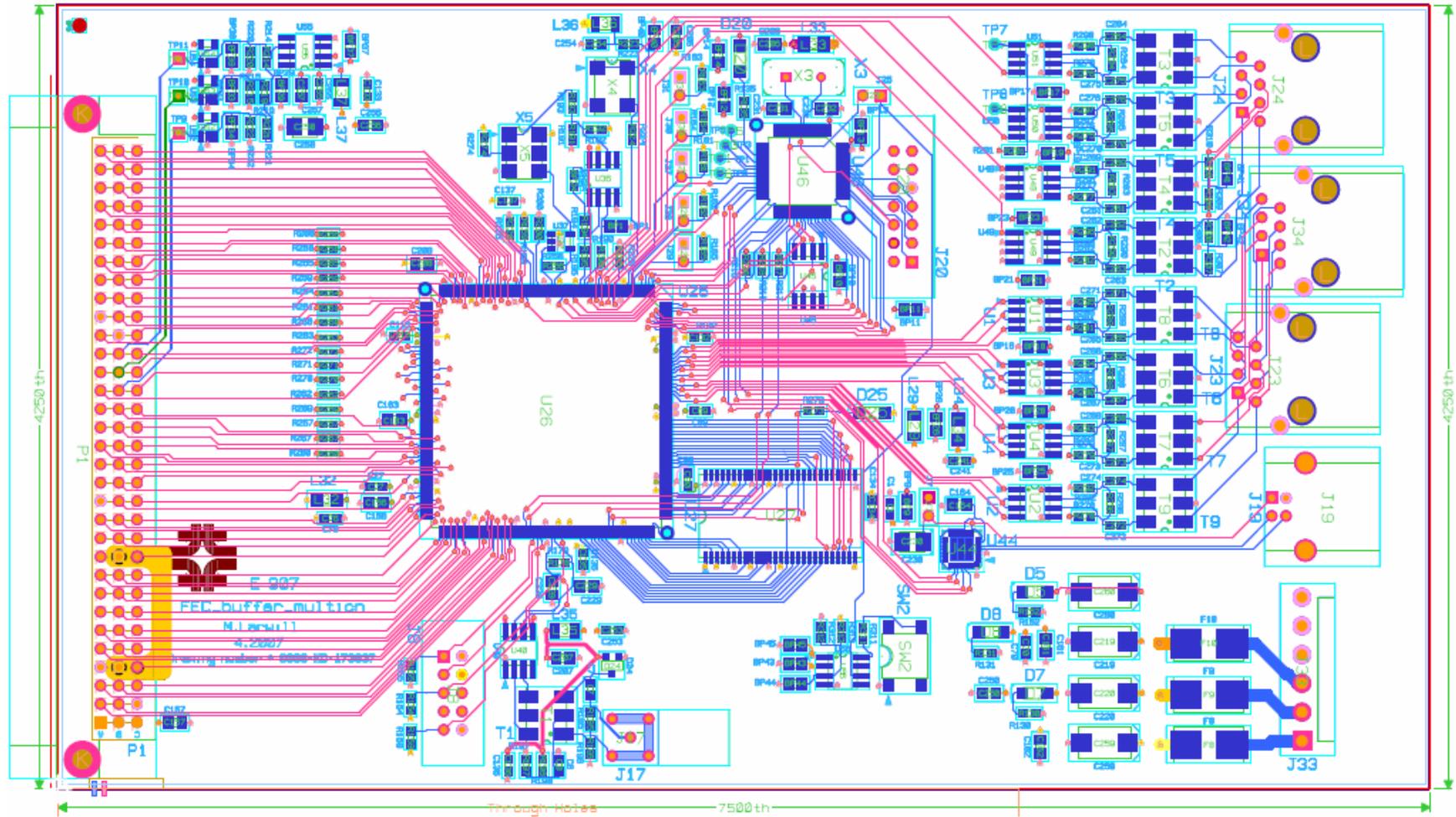
Mechanical design still needed for stick cooling.



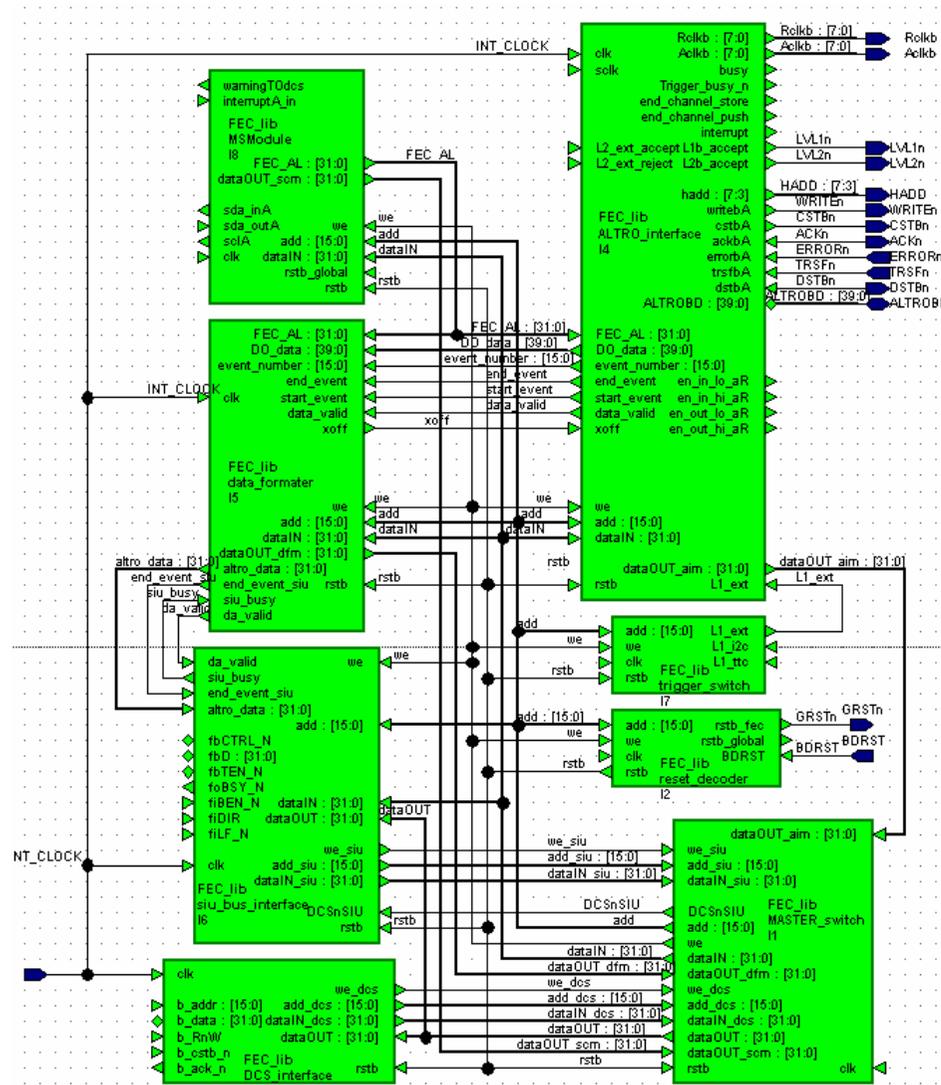
Schematic of Stick front end card buffer logic (Now with transformer coupled LVDS interface)



Layout of Stick front end card buffer logic for Pasa/Altro chip set



Block diagram of FPGA code for control logic of Pasa/Altro chip set



A simulation has been done using a VERILOG model of the ALTRO chip with code from the Alice front end design.

The simulation is working but additions for serial readout and multi event buffering are still being added.

Data format of Altro

The stream of zero-suppressed data must be formatted by adding, to each set of samples, two extra words, and encoding the 10-bit words and hardware address into a 40-bit set of words.

As it was mentioned in the previous paragraph, due to the removal of a variable number of samples between accepted clusters, the timing information would be lost during the zero-suppression process. This requires the addition of a time data to each accepted set of samples. Since 1000 is the maximum length of the data stream that can be processed by the ALTRO chip, the time information can be encoded in a 10-bit word. The principle is to label each sample with a time-stamp that defines the time distance from the trigger signal. So the samples of the processed data stream are numbered starting from 0 to 1000. The time information added to each cluster during the formatting phase corresponds to the time-stamp of the last sample in the cluster.

The ALTRO data format does not make use of extra flag bits to distinguish the samples data from the time data, but introduces a further word for each accepted cluster, which represents the number of words in the cluster without counting the time data.

These new 10-bit words, time data and number of samples per cluster, are introduced at the end of the cluster (fig 1.11).

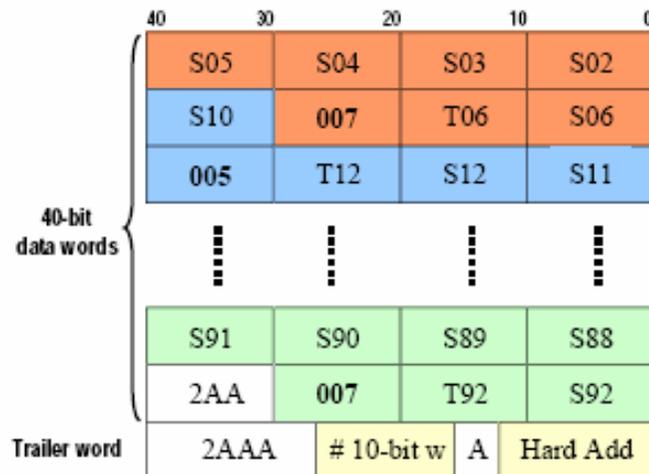


Figure 1.12. Back linked data block.

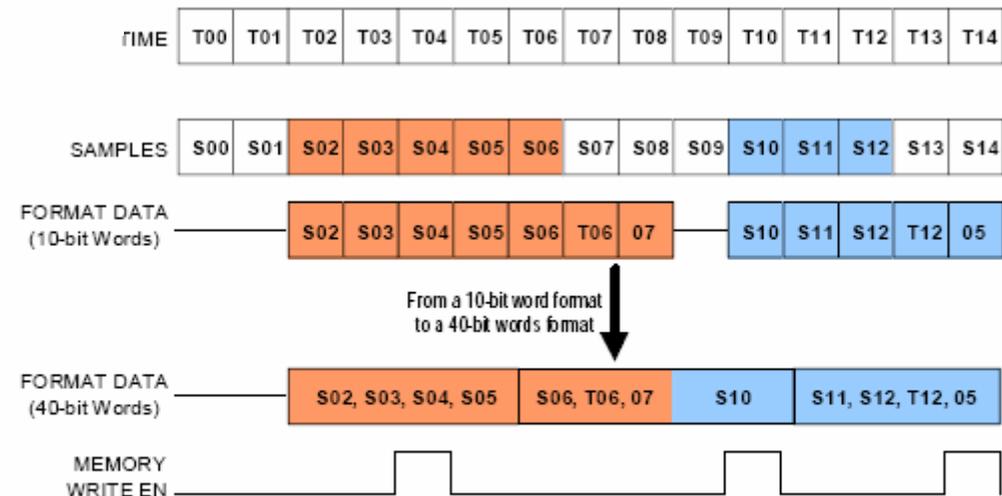
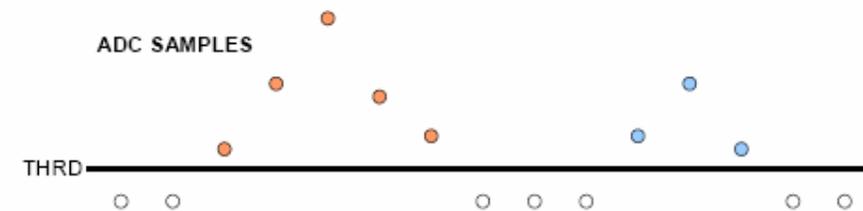


Figure 1.11. Data formatting procedure.

As it is shown in the fig 1.11 and fig 1.12, the 10-bit words are packed in 40-bit words. If some data is missing to complete a 40-bit word an "A" hexadecimal pattern is used. A

Multi Event Buffer

The processed data stream is stored in a memory to be eventually read out. This memory, 1024x40 bits wide, is partitioned in a programmable number N of blocks. Each data stream will be stored in the next available memory block. When all the memory blocks are occupied a full signal is generated to ignore the commands to process new data streams.

The number N of blocks can take the following 2 values: 4 and 8. The size of the memory allows storing 4 complete events without zero suppressed data. The way the data streams are sorted and recovered from the memory is completely transparent to the user. In any case the status of the memory (empty and full) is available in the chip status register.

Altro bus signals

The most relevant ALTRO bus signals are summarized in table 2.1. A more detailed description of the bus signals is given hereafter.

ALTRO BUS				
Signal Name	Function	# bits	Dir.	Polarity
AD	Address / Data	40	Bi-directional	H
WRITE	Write / Read	1	Input	L
CSTB	Command Strobe	1	Input	L
ACKN	Acknowledge	1	Output	L
ERROR	Error	1	Output	L
TRSF	Transfer	1	Output	L
DSTB	Data Strobe	1	Output	L
LVL1	Level-1 Trigger	1	Input	L
LVL2	Level-2 Trigger	1	Input	L
GRST	Global Reset	1	Input	L
SCLK	Sampling Clock	1	Input	-
RCLK	Readout Clock	1	Input	-

Table 2.1 Signal summary.

Altro bus data bits

AD[39:0] (bi-directional)

This is a 40-bit bi-directional Address/Data bus (table 2.2). It consists of three main fields that, starting from the least significant bit, are organised as follows: the *data* field (20 bits), the *instruction* field (5 bits) and the *address* field (14 bits). The most significant bit is a parity bit. It should be noted that, with a 14-bit *address* field, the ALTRO bus space sizes 16384. This addressable space is divided in two equal size partitions: the ALTRO chips partition (AL partition) and the Board Controller partition (BC partition).

	39	38	37	36	29	28	25	24	20	19	0
PAR	ADDRESS						INSTRUCTION CODE			DATA	
	BCAST	BC/AL	CHANNEL ADDRESS								

Table 2.2: 40-bit bi-directional Address/Data bus

AD[39] (PAR) is the parity bit of the 20 most significant bits. It is set such that the parity of the 20 most significant bits is always even. The parity bit allows the detection of a single bit error in the transmission between the RCU and the FEC.

When the bit AD[38] BCAST (broadcast) is set to 1, the *bus write cycle* initiated by the RCU (master) is addressed to an entire *partition* of the *address space* (AL or BC partition). In this case the slave units ignore the channel address field.

The bit AD[37] (BC/AL) defines the address space partition: 1 for the BC partition, 0 for the AL partition.

The following 8 bits AD[36:25] (CHANNEL ADDRESS) specify the *channel address* and, during an *instruction cycle*, are compared with the hard-wired address. From the most significant bit, the channel address consists of a branch address (1 bit), the FEC address

(4 bits), the ALTRO chip address (3 bits) and the ALTRO's internal channel address (4 bits). This allocations of addresses is the recommended one and it corresponds to the case of a board containing 8 ALTROs (FEC) and an RCU with two branches each one with 16 FECs.

Altro Registers

Per Channel Registers					
Reg. Name	Reg. Add.	Width	Access Type	Allow Bcast	Meaning
K1	00	16	R/W	Y	Filter Coefficient K1
K2	01	16	R/W	Y	Filter Coefficient K2
K3	02	16	R/W	Y	Filter Coefficient K3
L1	03	16	R/W	Y	Filter Coefficient L1
L2	04	16	R/W	Y	Filter Coefficient L2
L3	05	16	R/W	Y	Filter Coefficient L3
VFPED	06	20	R + R/W	Y	Variable / Fixed Pedestal Data
PMDTA	07	10	R/W	Y	Ped. Mem. Data for a given address
ADEVL	11	16	R	N/A	Chip Address + Event Length

The total number of registers implemented in the ALTRO chip is 137. Out of these 128 are channel specific. That is, a different version exists for each channel. These are 8 channel-specific registers for each of the 16 channels (8x16= 128)

The remaining 9 registers contain parameters that are either common for all the channels or relative to the common logic of the chip.

The PMD register is not a true register, but a gateway to access the pedestal memories.

Global Registers					
Reg. Name	Reg. Add.	Width	Access Type	Allow Bcast	Meaning
ZSTHR	08	20	R/W	Y	Offset + Threshold ZS
BCTHR	09	20	R/W	Y	Threshold HI + Threshold LO (MAU)
TRCFG	0A	20	R/W	Y	Trigger Delay + N. Samples/Event
DPCFG	0B	20	R/W	Y	ZSU + MAU + BSU configuration
BFNPT	0C	5	R/W	Y	Filter Enable + Buffer. N. + Pre-trigger
ERSTR	10	20	R	N/A	Error + Status Register
TRCNT	12	16	R	N/A	Trigger Counter
PMADD	0D	10	R/W	Y	Pedestal Memory Address

Altro command set

Command Set				
Reg. Name	Reg. Add.	Access Type	Allow Ibroadcas	Meaning
WPINC	18	W	Y	Write Pointer Increase
RPINC	19	W	Y	Read Pointer Increase
CHRDO*	1A	W	N	Channel Readout
SWTRG	1B	W	Y	Software Trigger
TRCLR	1C	W	Y	Clear Trigger Counter
ERCLR	1D	W	Y	Clear Error Flags

Table 2.4. Command set.

Readout Command

The data dump takes place immediately after the acknowledging of the readout command. The execution of this command does not involve the SCLK at all, therefore the timing is fixed relative to the readout clock. Fig. 2.3 sketches the timings for the Readout command.

Basic timing. The $\overline{\text{CSTB}}$ and $\overline{\text{WRITE}}$ lines must be held low until $\overline{\text{ACK}}$ is asserted. The upper data lines must be valid during the assertion of $\overline{\text{CSTB}}$. Three clock cycles after the de-assertion of $\overline{\text{ACK}}$ the chip will start driving the 40 data lines. On the following clock cycle, $\overline{\text{TRSF}}$ will be asserted and output data will be valid on each falling edge of $\overline{\text{DSTB}}$. One clock cycle after the de-assertion of $\overline{\text{TRSF}}$ the data bus will be in high impedance.

