

# TPC electronics Status, Plans, Needs

Marcus. Larwill  
Dec. 2006

Many of the following slides were taken from  
previous talks about MIPP or ALICE  
Pasa/Altro and are not totally my creation

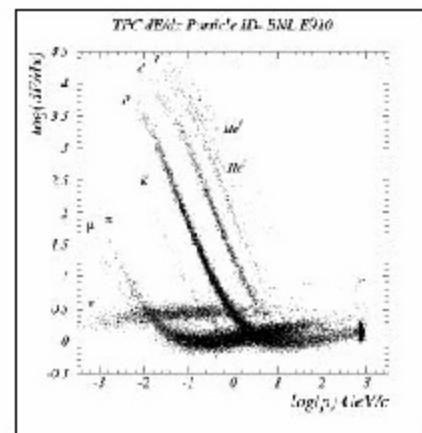
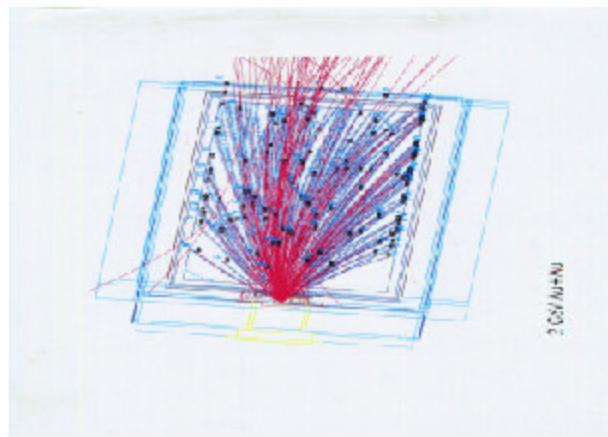
# Short list of topics

- Why the Pasa/Altro
- Mipp TPC data path requirements
- Lessons learned from previous TPC Sticks
- Review of previous Pasa/Altro Layouts
- Design and layouts of new Sticks
- Power , Thermal and other limitations.

## MIPP- TPC

- This Time Projection Chamber, built by the BEVALAC group at LBL for heavy ion studies currently sits in the E-910 particle production experiment at BNL, that has completed data taking. It took approximately \$3million to construct.
- Can handle high multiplicity events. Time to drift across TPC=16  $\mu$ s.
- Electronic equivalent of bubble chamber, high acceptance, with dE/dx capabilities. Dead time 16 $\mu$ s. i.e unreacted beam swept out in 8 $\mu$ s. Can tolerate  $10^5$  particles per second going through it.
- Can handle data taking rate ~60Hz with current electronics. Can increase this to ~1000 Hz with an upgrade.
- TPC dimensions of 96 x 75 x 150 cm.

*TPC*



Aug 22, 2005

Rajendran Raja, Snowmass 05

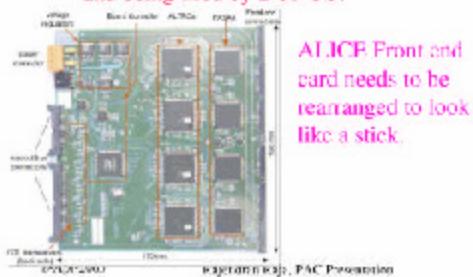
27

## *MIPP Upgrade program*

- Speed up TPC DAQ by using ALICE ALTRO/PASA chips. We have been given the green light to acquire these chips from CERN (\$80K).
- Speed up rest of DAQ.

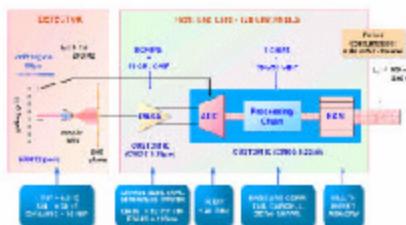
## ALICE PASA/ALTRO Chip

- PASA-Preamplifier/Pulse shaper One chip=16 pads.
- ALTRO-Digitizes, memory buffer. Controlled by ALTRO bus (40bits wide) with a Readout Control Unit.
- Thoroughly debugged and tested for ALICE. Needed by STAR, TOTEM, MIPP and being used by BONUS.

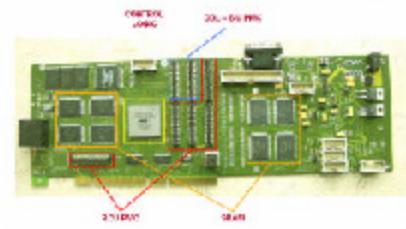


40

## ALTRO/PASA chips



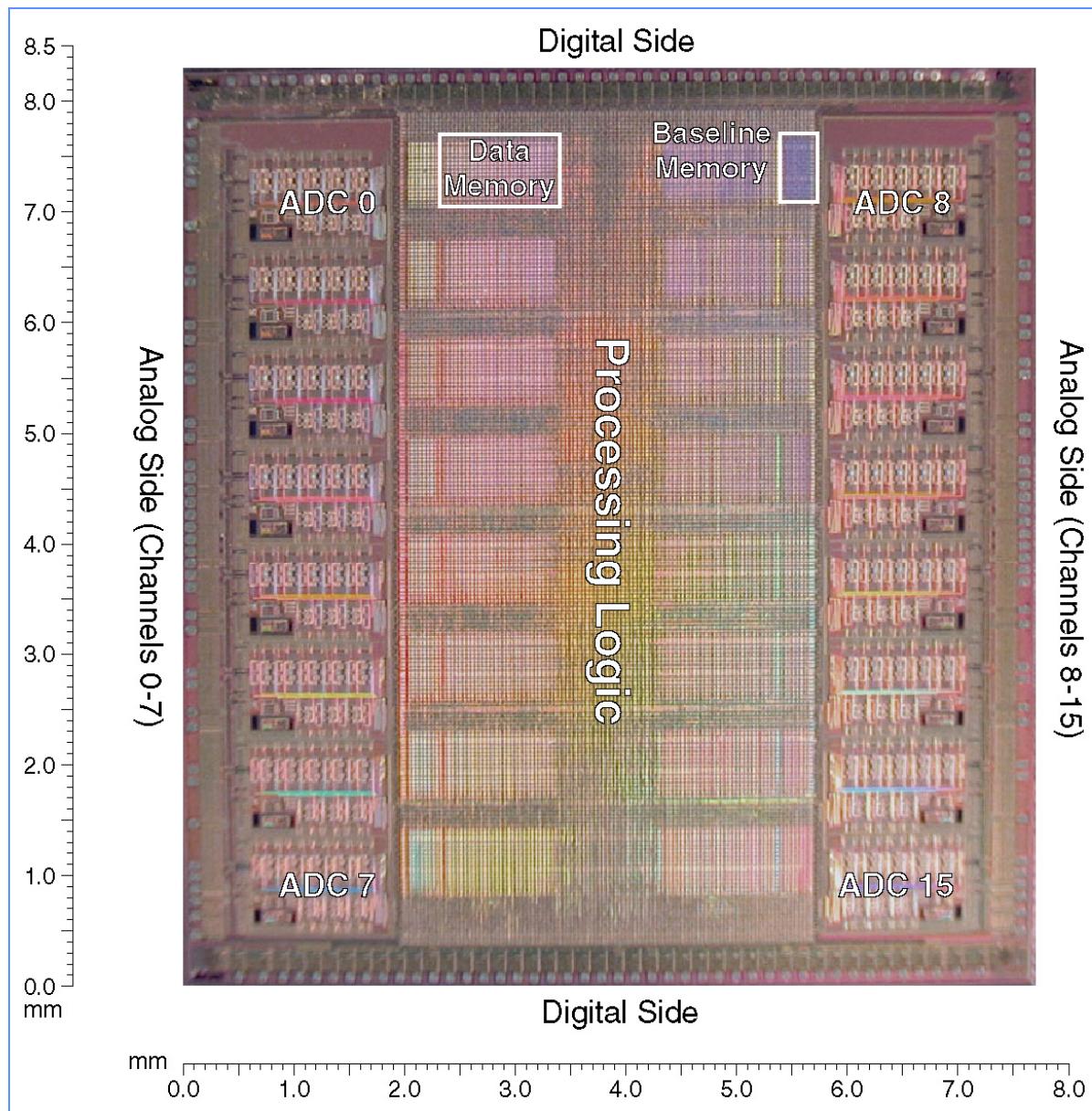
### RCU Prototype II



6-Aug-2005

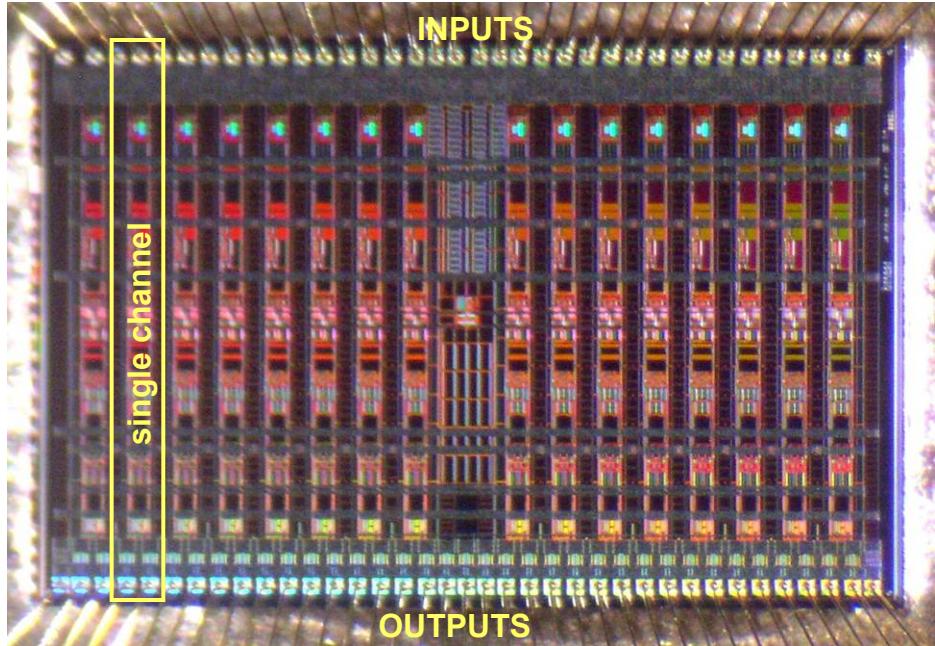
Rajendran Raja, PAC Presentation

41



<b>Process</b>	HCMOS-7 (0.25 $\mu$ m)
<b>Area</b>	64 mm <sup>2</sup>
<b>Transistors</b>	6 millions
<b>Embedded memory</b>	800 kbit
<b>ENOB</b>	9.7
<b>Power</b>	16mW / channel

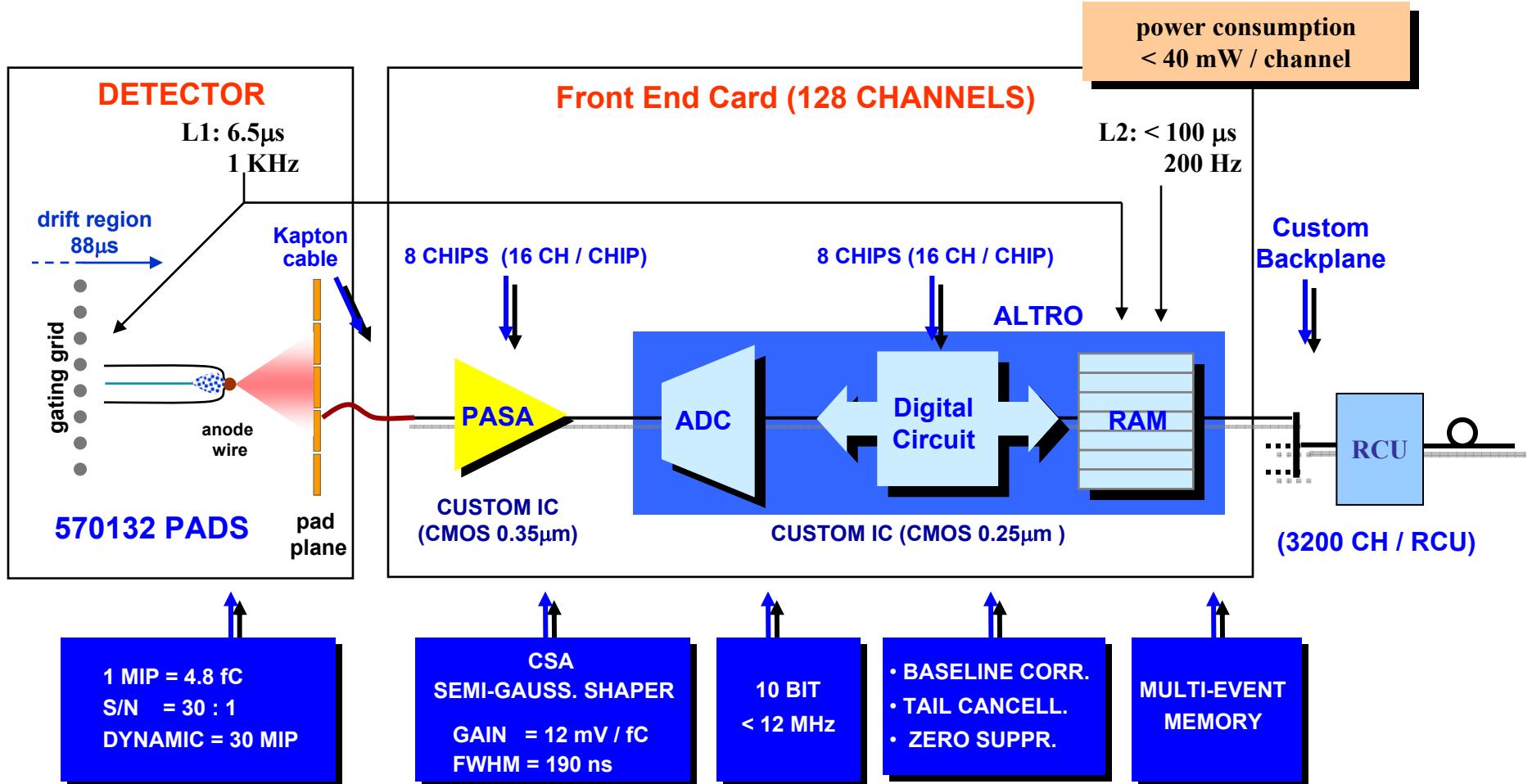
<b>ER (4K chips)</b>	Apr '02
<b>Mass prod. (44K chips)</b>	Dec '02
<b>Mass test</b>	Feb '04
<b>Yield</b>	84%



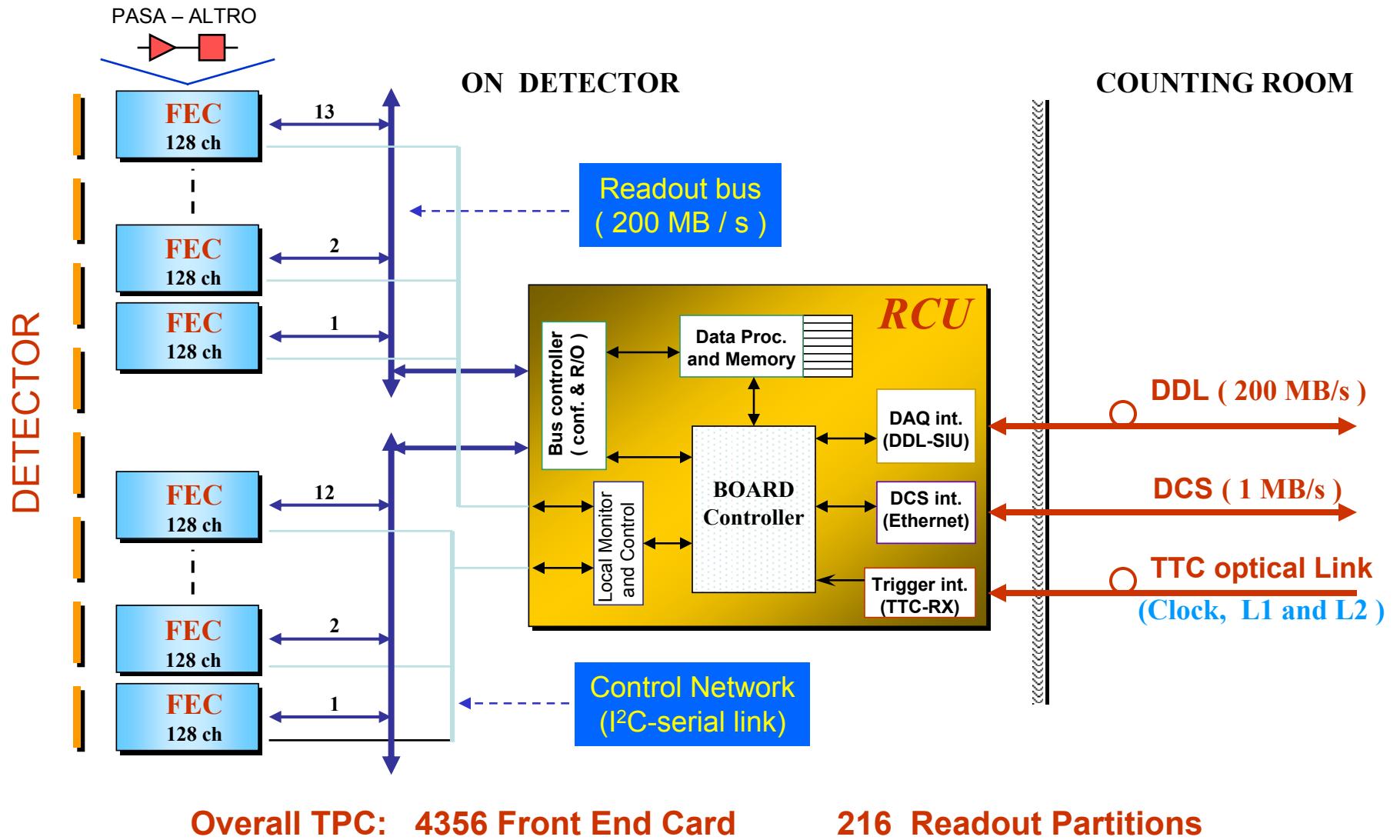
## Production Engineering Data

- process: AMS CMOS 0.35  $\mu\text{m}$
- area: 18 mm<sup>2</sup>
- MPR samples: Jan '02
- ER samples (500 chips): Sep '03
- full delivery (49359 chips): Jan '04
- Completion of mass test: May '04
- yield (working chips): 94%
- yield = 83% : |CG| < 5%, |PT|<5%, |BSL| < 5%

Parameter	Requirement	MPR Version	Production
Noise	< 1000e	566e (@12pF)	560e (12pF)
Conversion gain	12mV / fC	10.8mV / fC	12mV / fC
Shaping time	190ns	190ns	188ns
Non linearity	< 1%	< 0.35%	0.2%
Crosstalk	<0.3%	0.4%	< 0.1%
Gain dispersion		~1%	2% (r.m.s.)
Power consumption	< 20mW	12mW / ch	11mW / ch



## Each of the 36 TPC Sectors is served by 6 Readout Partitions

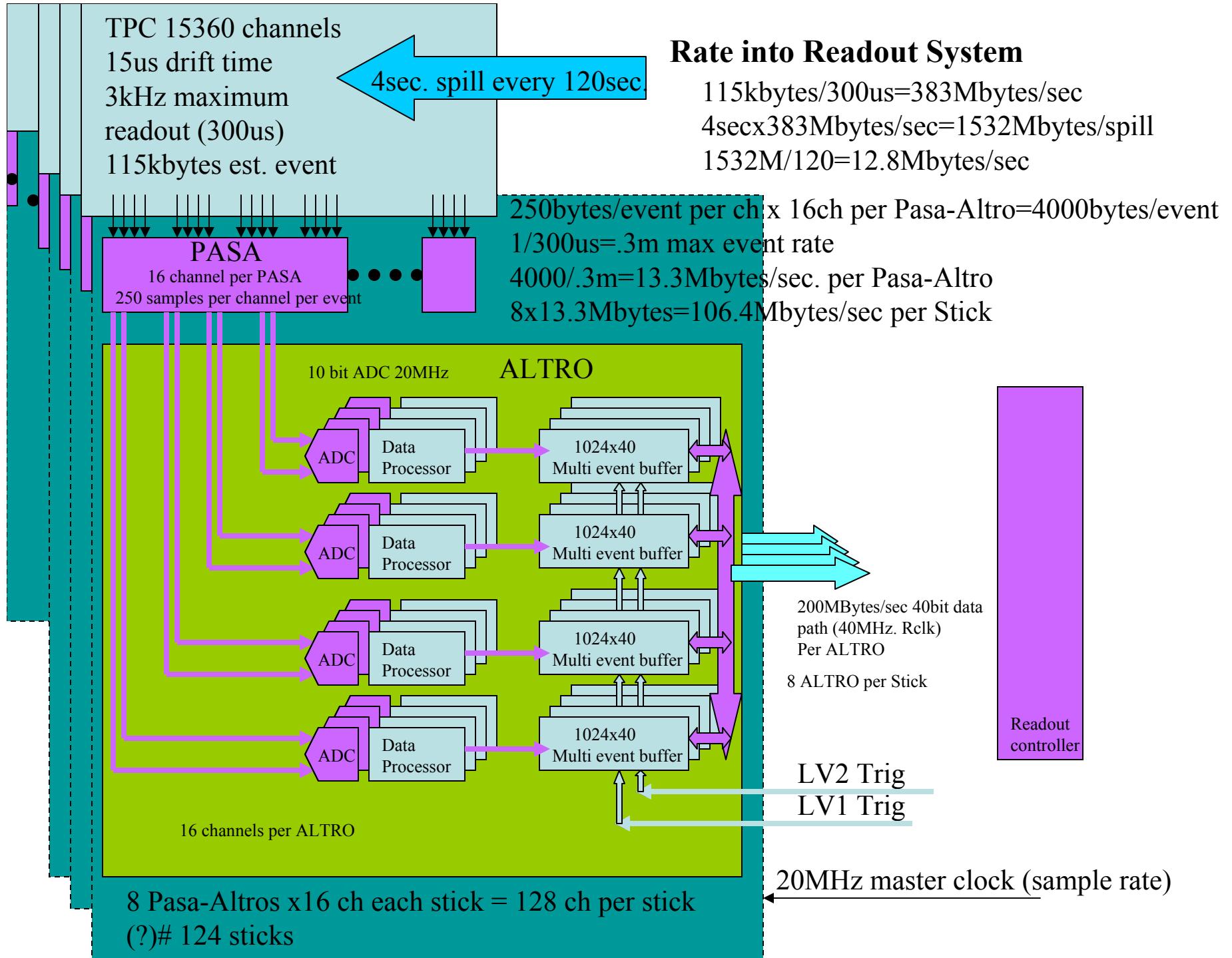


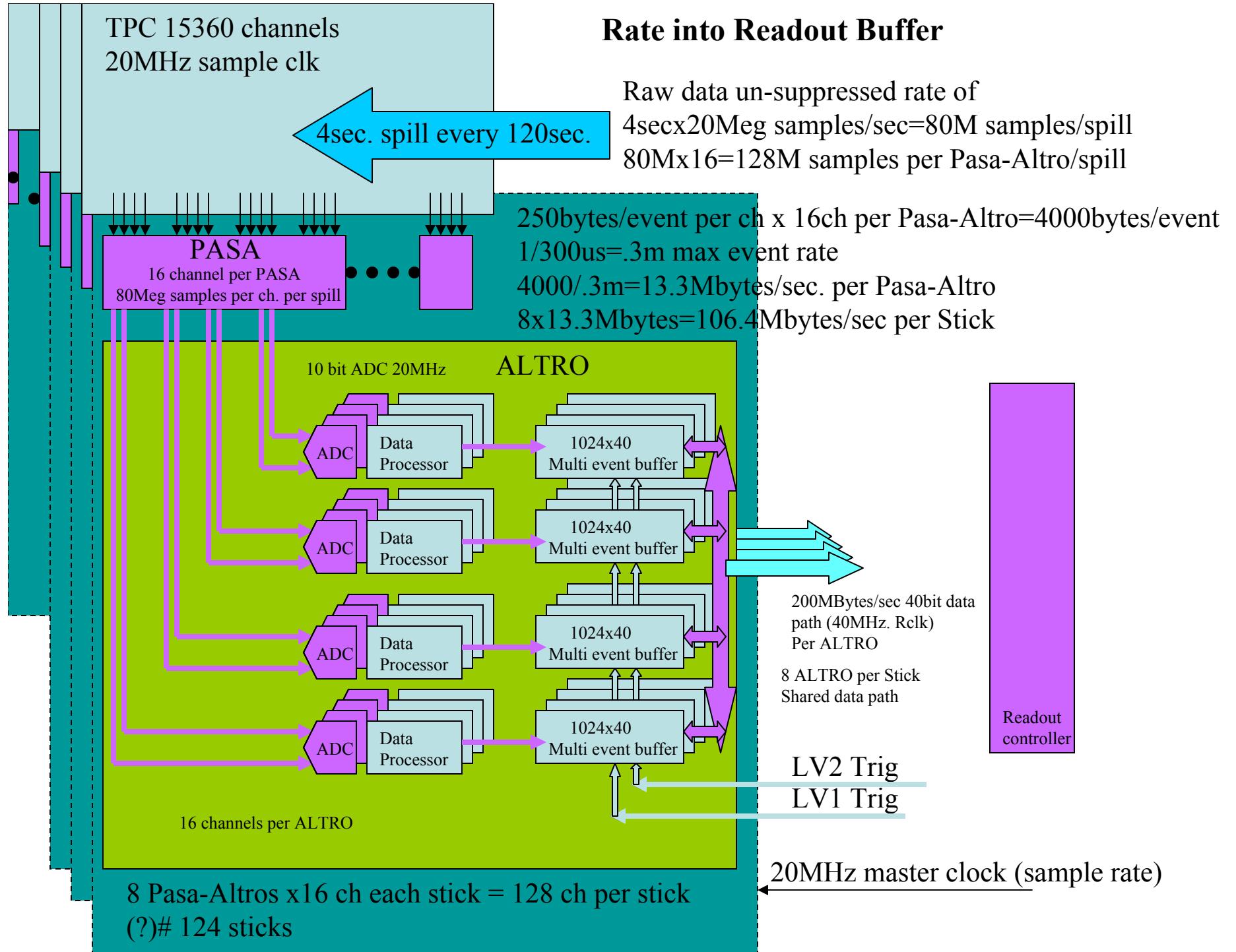
# Data Path Requirements of TPC

- The SY120 program will switch to one 4 second slow spill every 2 minutes.
- The gaseous volume drift height is 75cm, corresponding to a maximum collection time of 15usec.
- The TPC grid is currently limited to a maximum pulse rate of 3kHz.
- The readout should be capable of a sustained rate of .3ms per event and a burst rate of .2ms per event.
- The 15360 channels of TPC are used to measure particle trajectory momentum and dE/dx.
- The detector is currently instrument with 128 analog/digital electronics cards “sticks” which would be designed to have PASA/ALTRO chips.  $15360/128=120$
- For the TPC there will be 250 samples per event channel to match the drift time of the detector.
- With a zero suppressed event size estimated to be 115kb for multi track events.

# Data Path of TPC

- A 575mb/s burst rate readout could be achieved with 5-way parallel 115mb/s datapaths.
- Each PASA/ALTRO chip sets has a 10bit 40MHz. ADC, with digital signal processor and memory buffer.
- The chips are controlled over a 40bit wide bus that supports 200MB/s.
- The ALTRO event buffer will be able to fully buffer 8 events.





## What can be learned from E907 Front End Cards (Sticks)

The 128 front-end cards, known as “sticks,” sit in the electronics bay just below the pad plane.

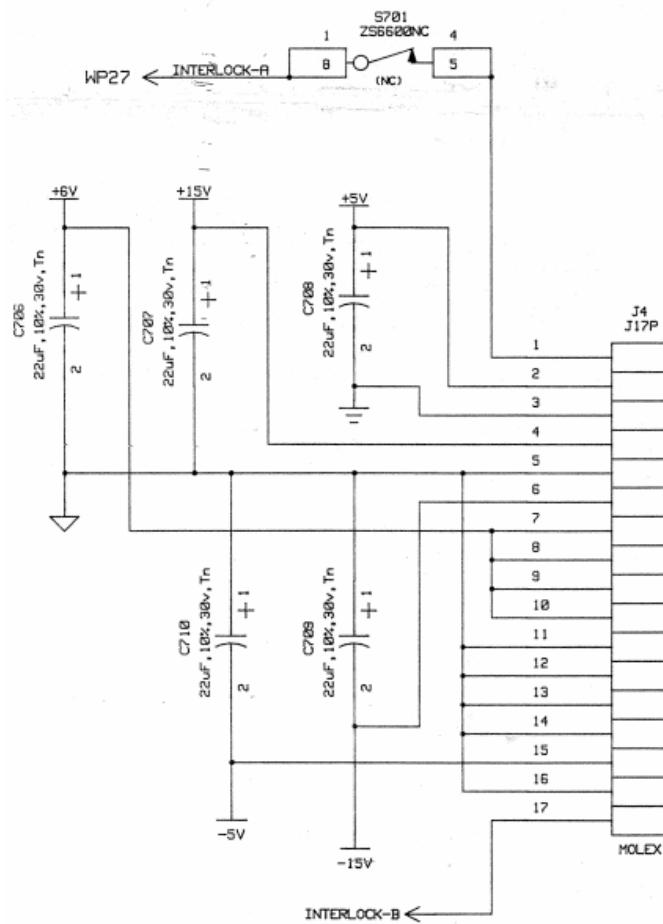
There are on-board power and interlock connections.

The sticks are constructed of two multi-layer boards mounted on a thin aluminum wedge. When installed, the base of the wedge is in contact with the bottom of the electronics bay, which is water-cooled. This is the primary cooling for the sticks.

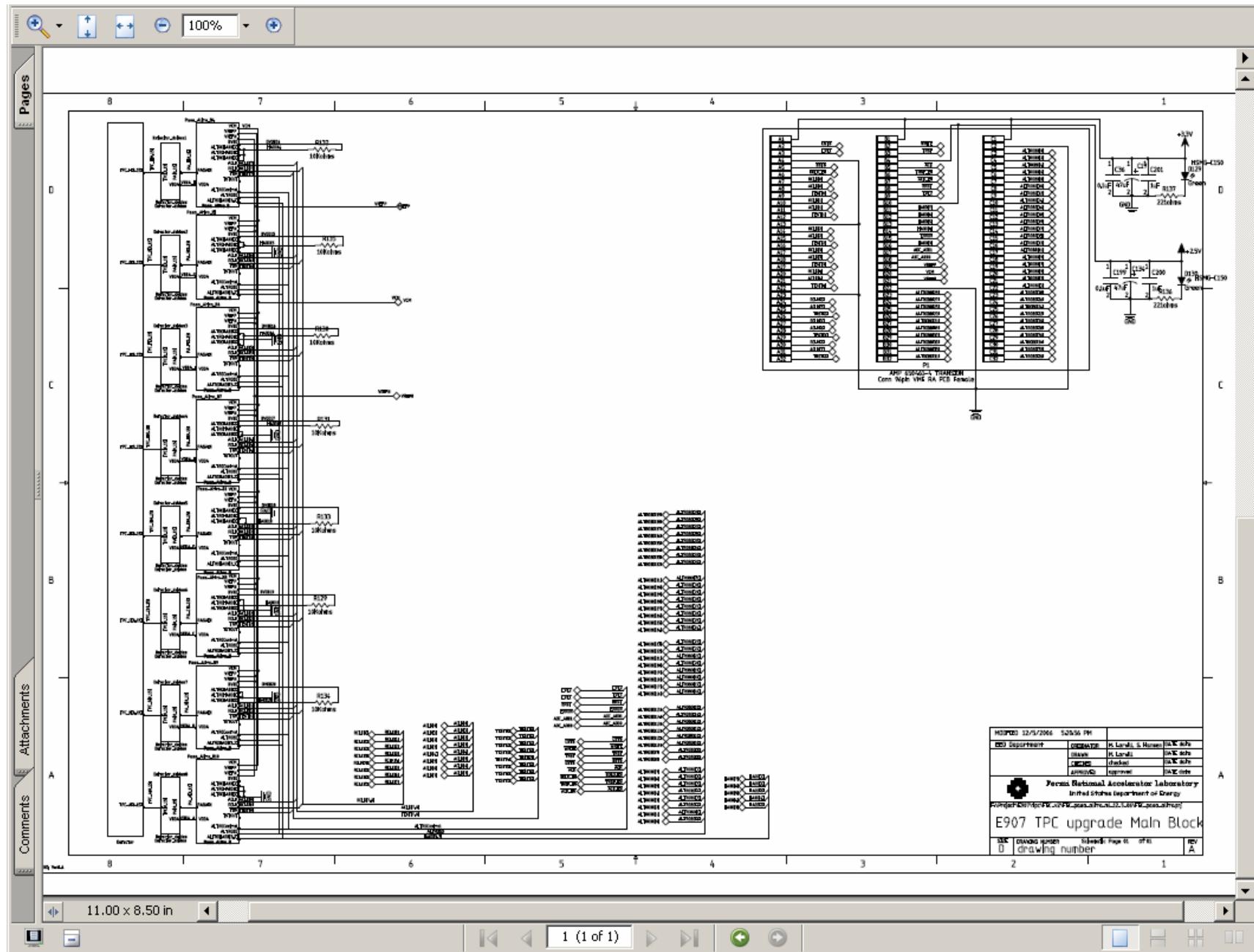
The electronics bay is purged with nitrogen. The exhaust passes a smoke detector on the AC interlock loop.

The sticks connect to the pad plane structure through a zero-insertion-force card edge connector (essentially an [AMP Linear ZIF Connector](#)). The pad plane and ZIF connector, in addition to connecting the pads to the sticks, encode the stick slot position and form an interlock for proper card insertion. If the card is not completely inserted, the interlock contacts are not made up, and the DC power supply interlock will not make up for that stick, preventing power from being applied to the board. The sticks also contain a thermal limit switch, set to open at 40°C, in the interlock chain.

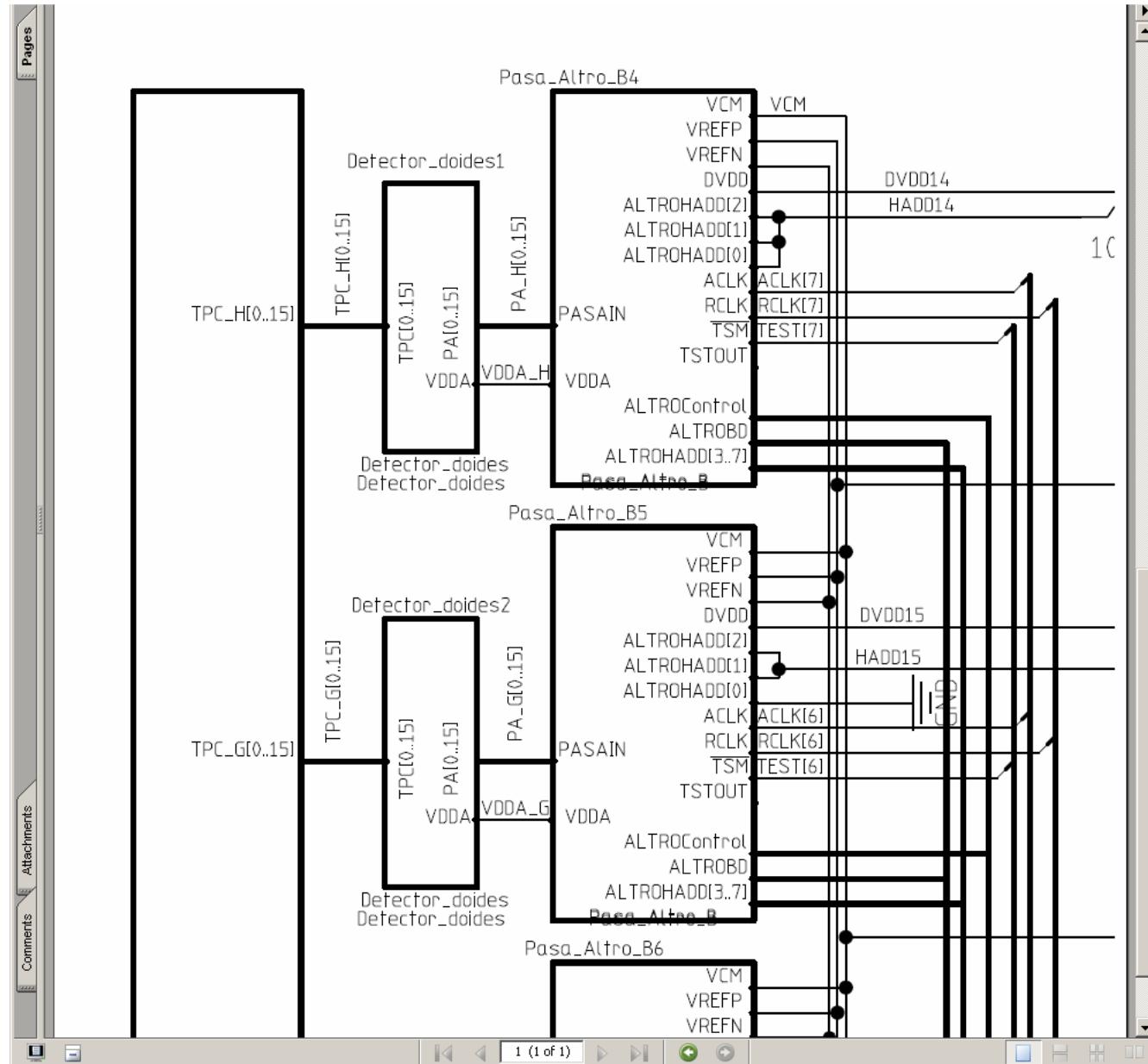
The sticks are supplied  $\pm 15$  V,  $\pm 5$  V, and +6 V DC power through a 17-pin Molex connector. In addition, each stick receives two 10-pin ribbon cables, one for the slow control BitBus interface, the other for clock and trigger distribution. Finally, the digitized data are pushed out onto optical fiber using a Taxi chip.



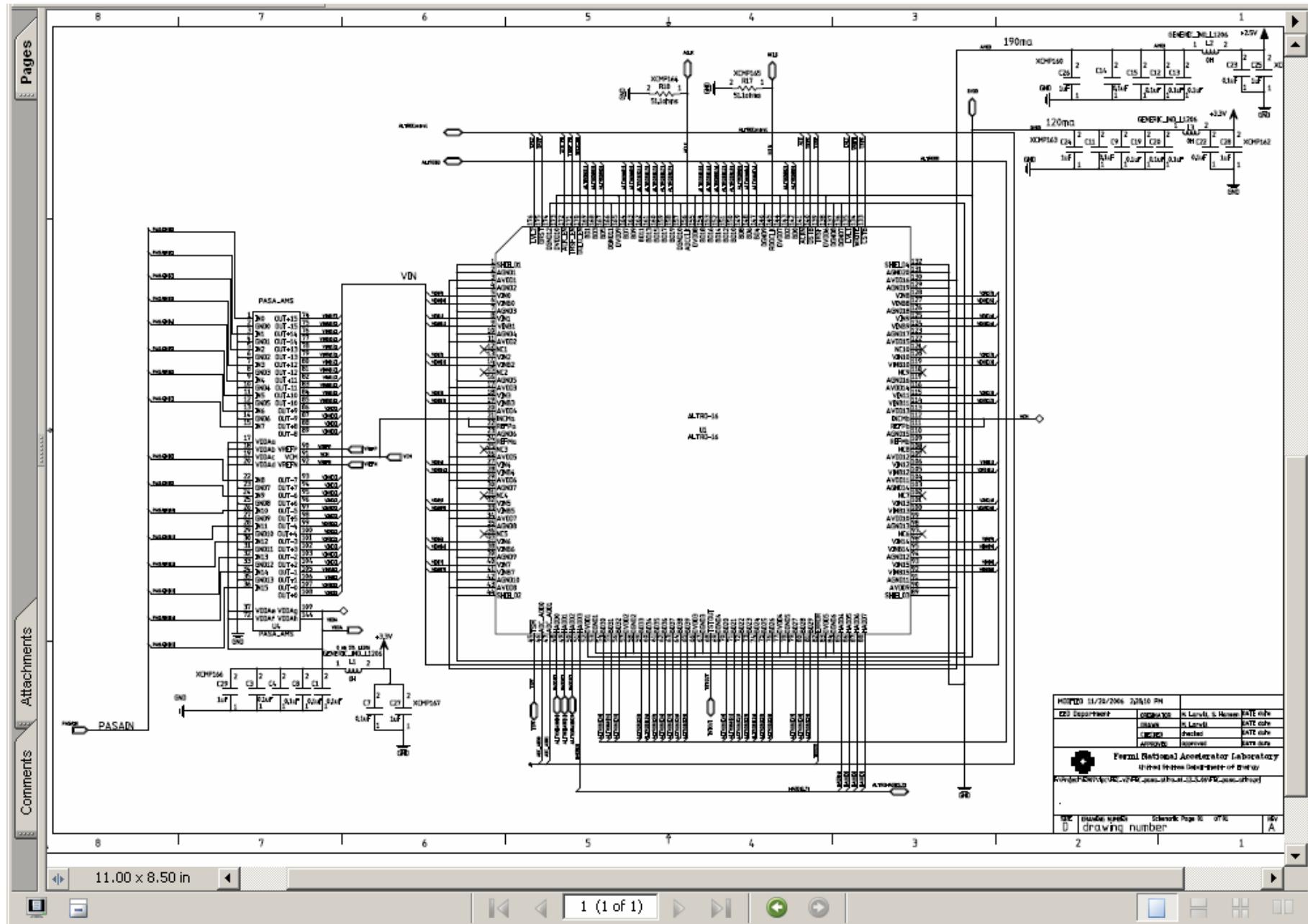
# Prototype Top level schematic of Altro/Pasa chips on Stick for Mipp



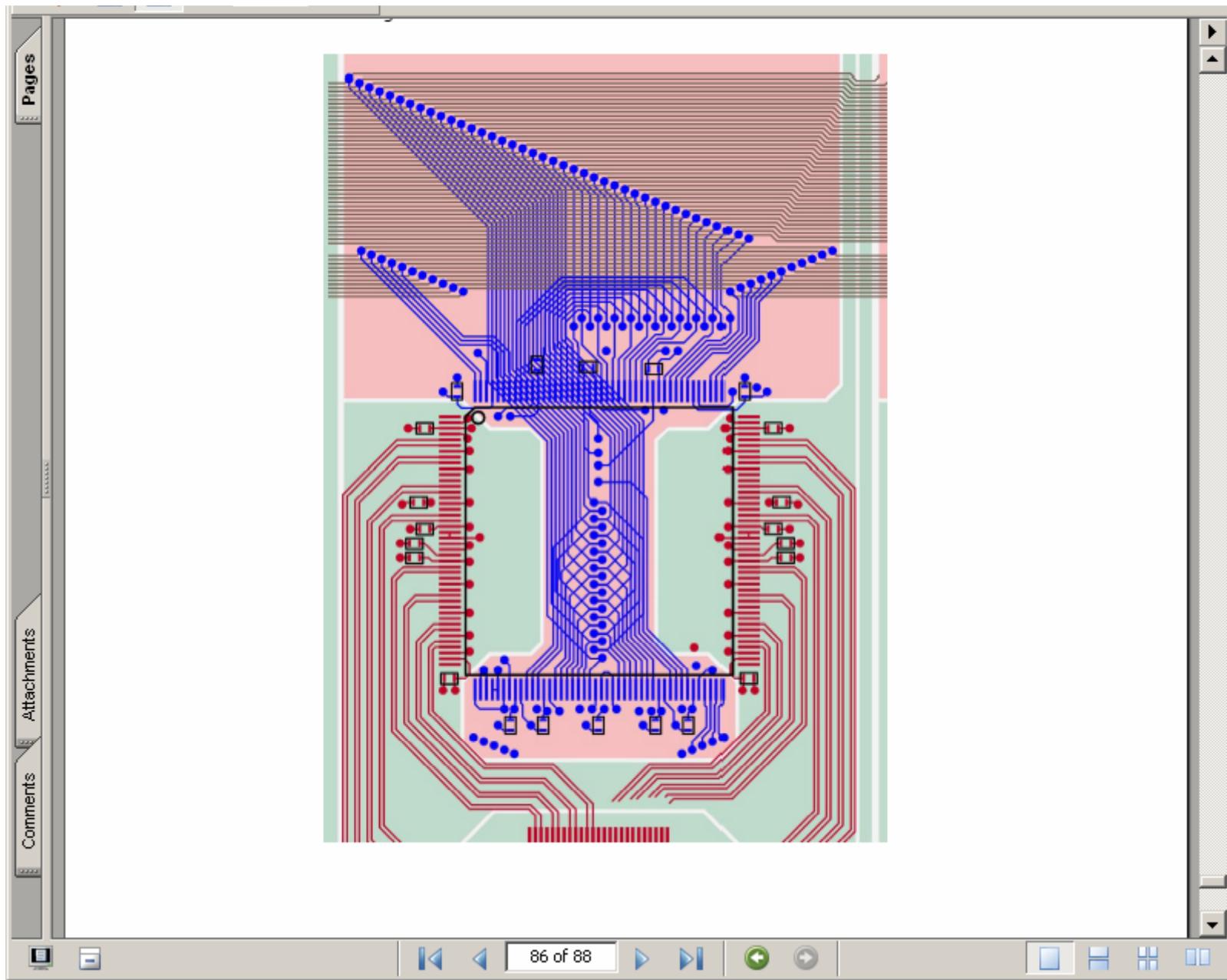
# Close up of Prototype schematic



# Schematic of Pasa/Altro chip set

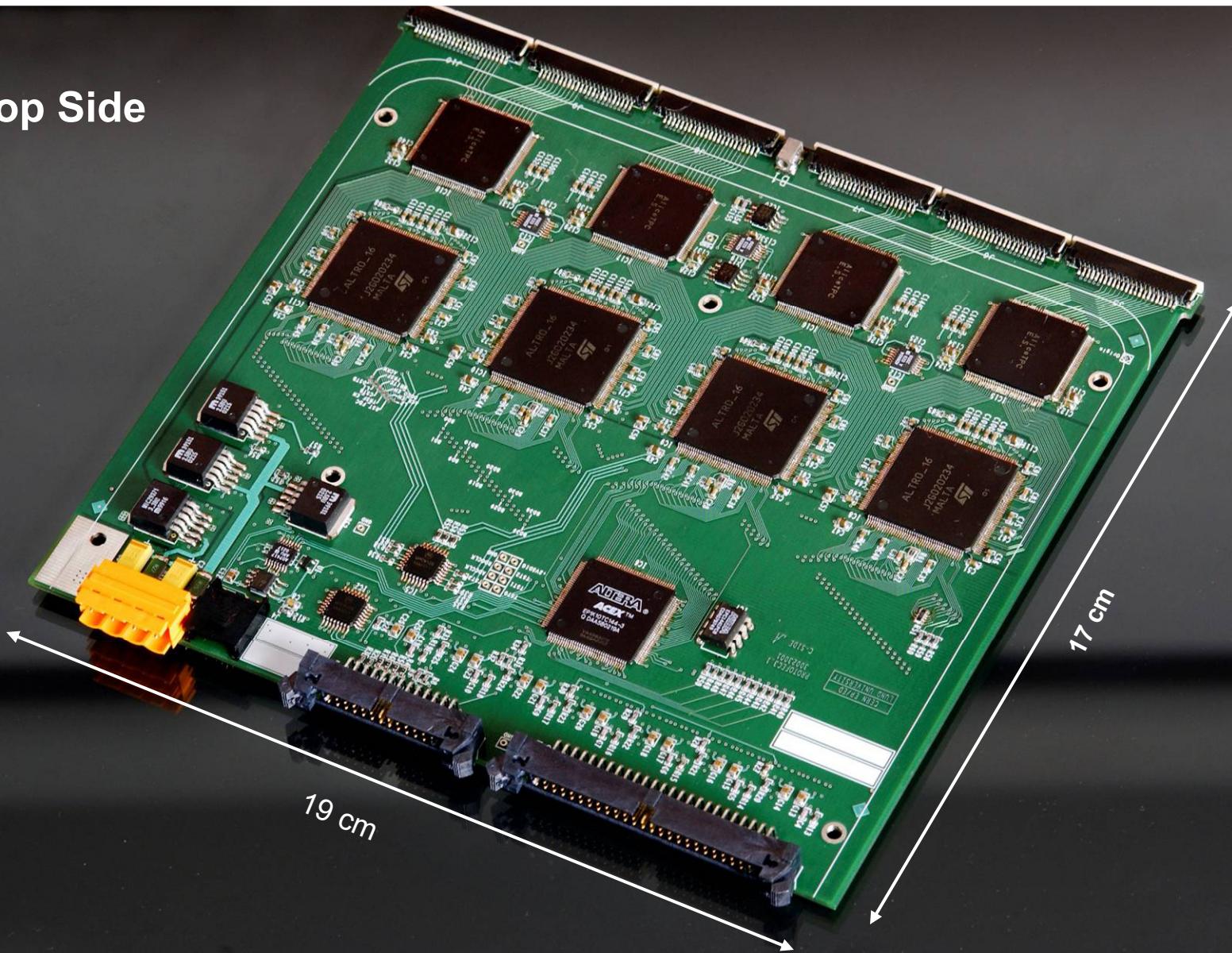


## Recommended layout of Pasa/Altro chip set

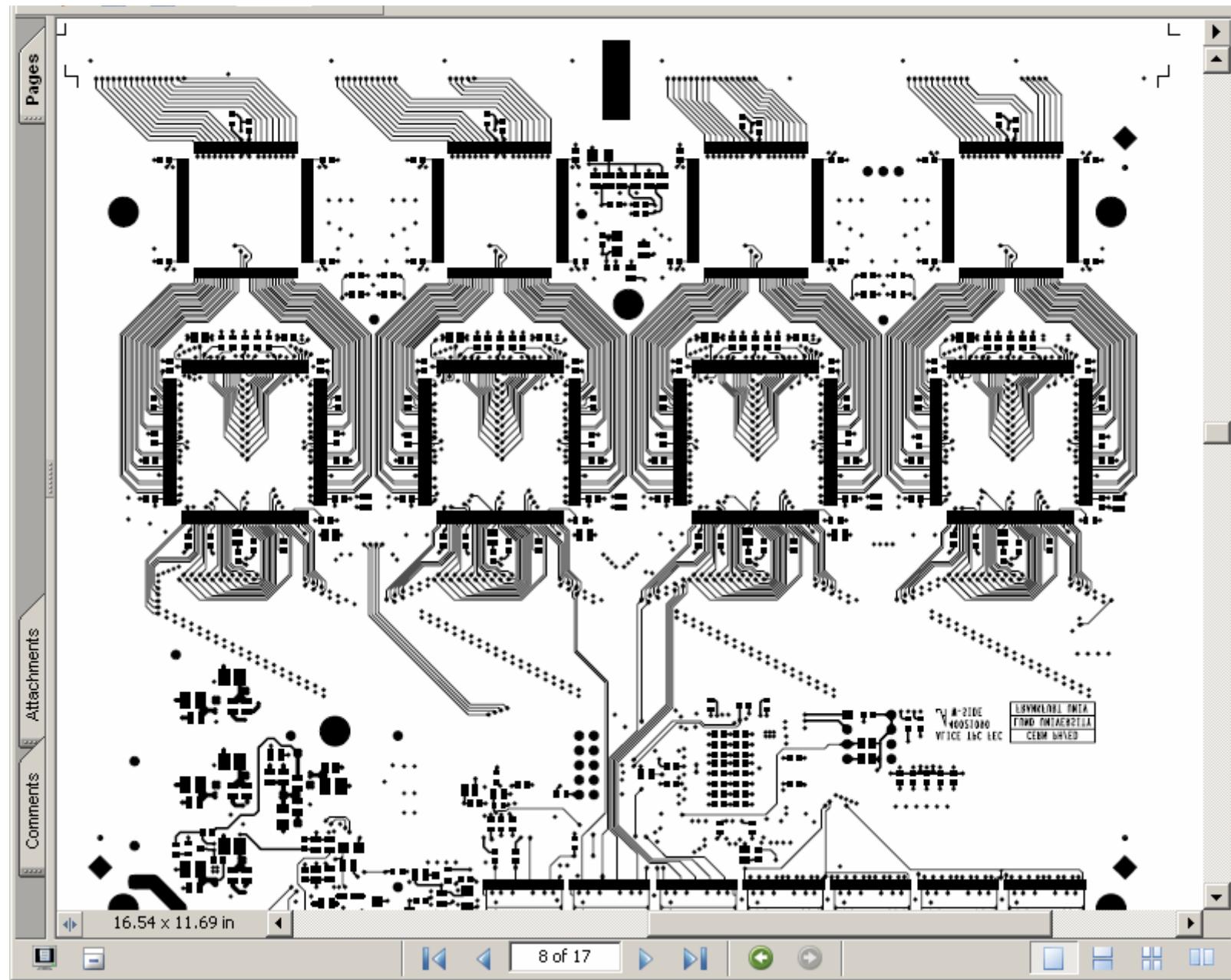


Close up of Alice front end card with Pasa/Altro chip set

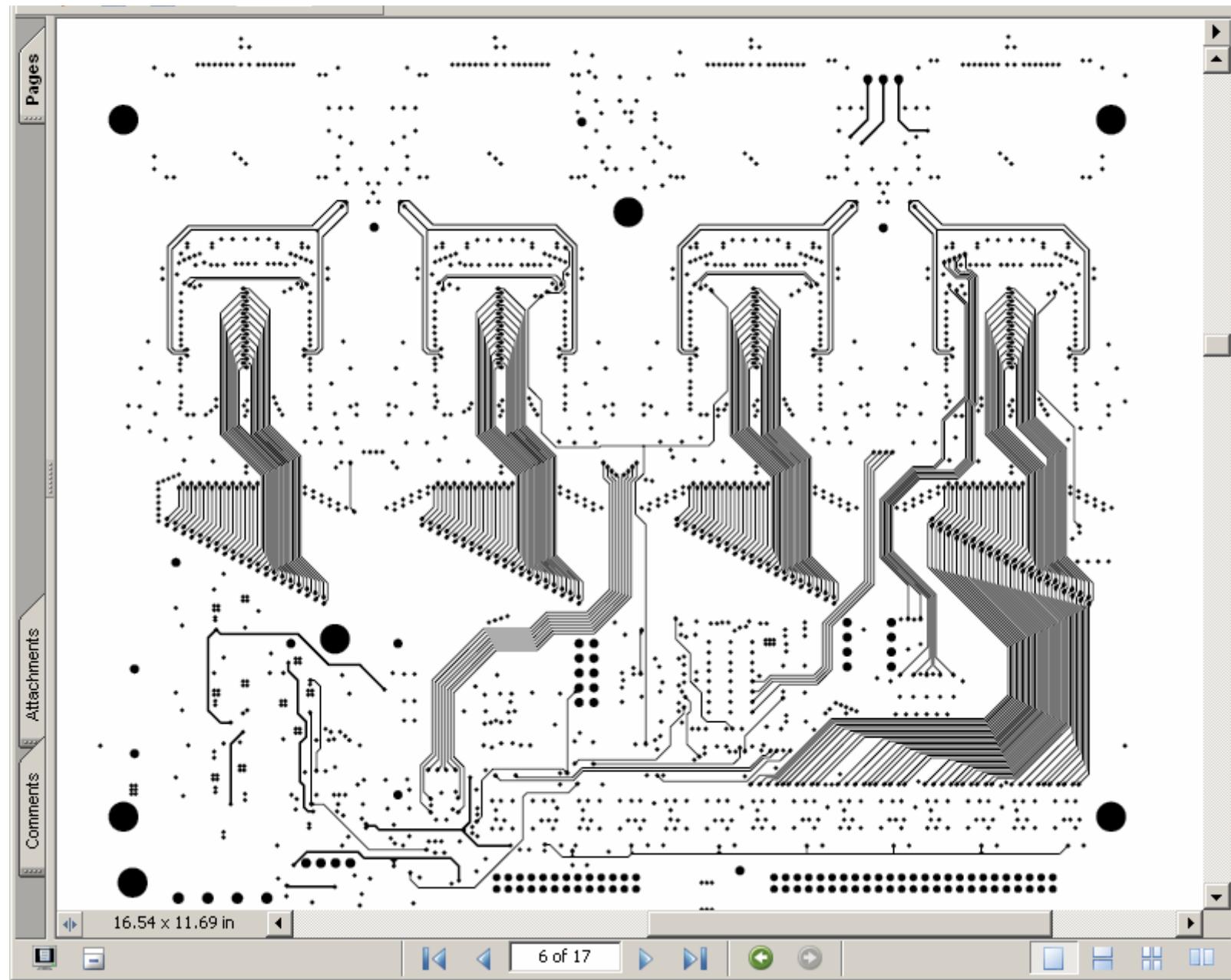
Top Side



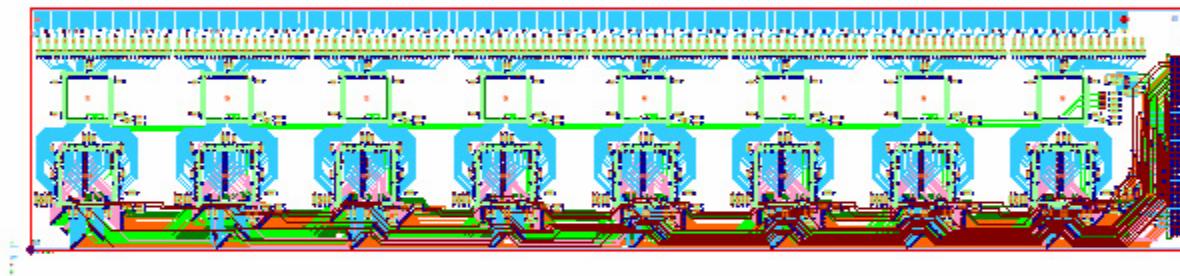
## Close up Layout of Alice front end card with Pasa/Altro chip set



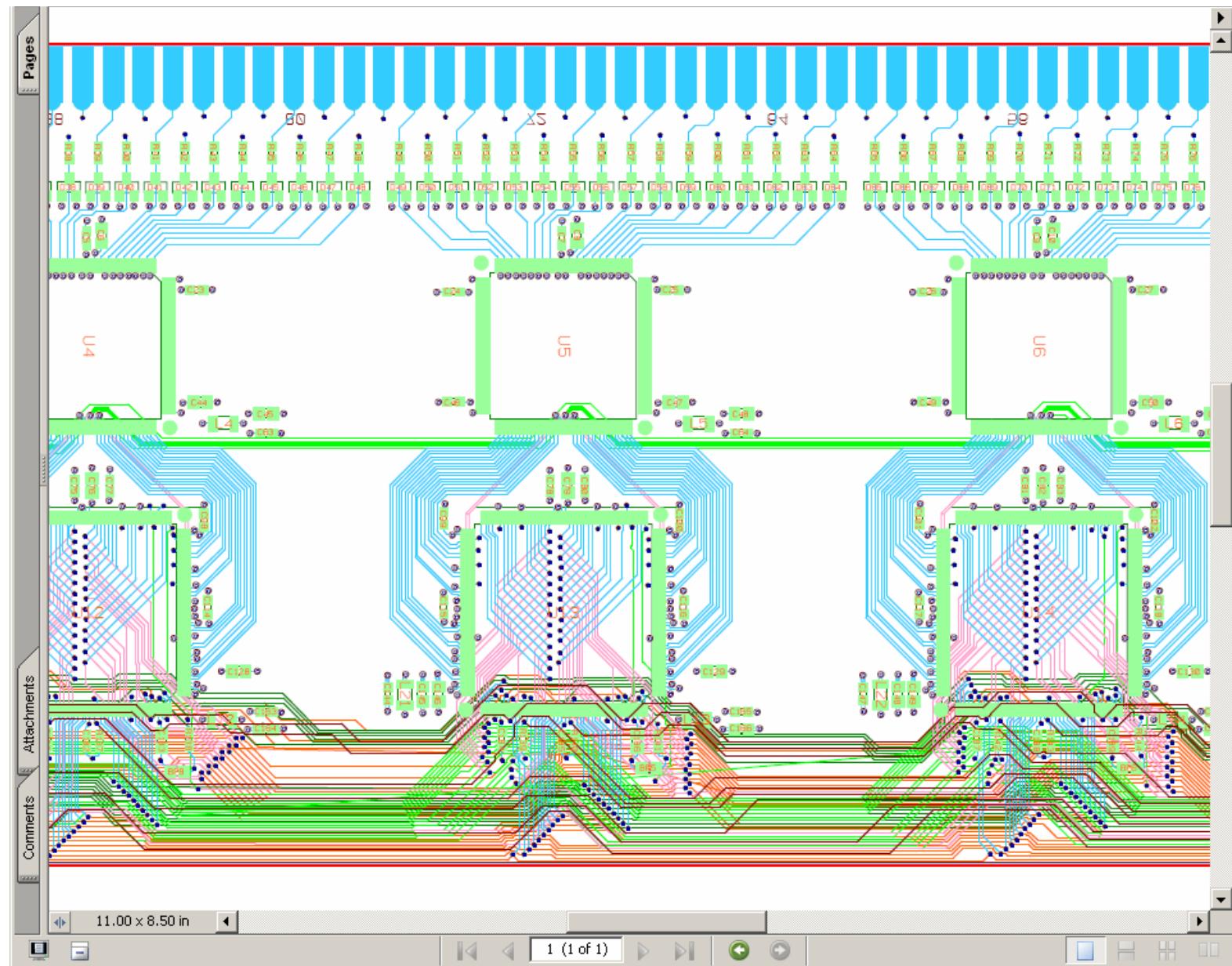
## Close up Layout of Alice front end card with Pasa/Altro chip set



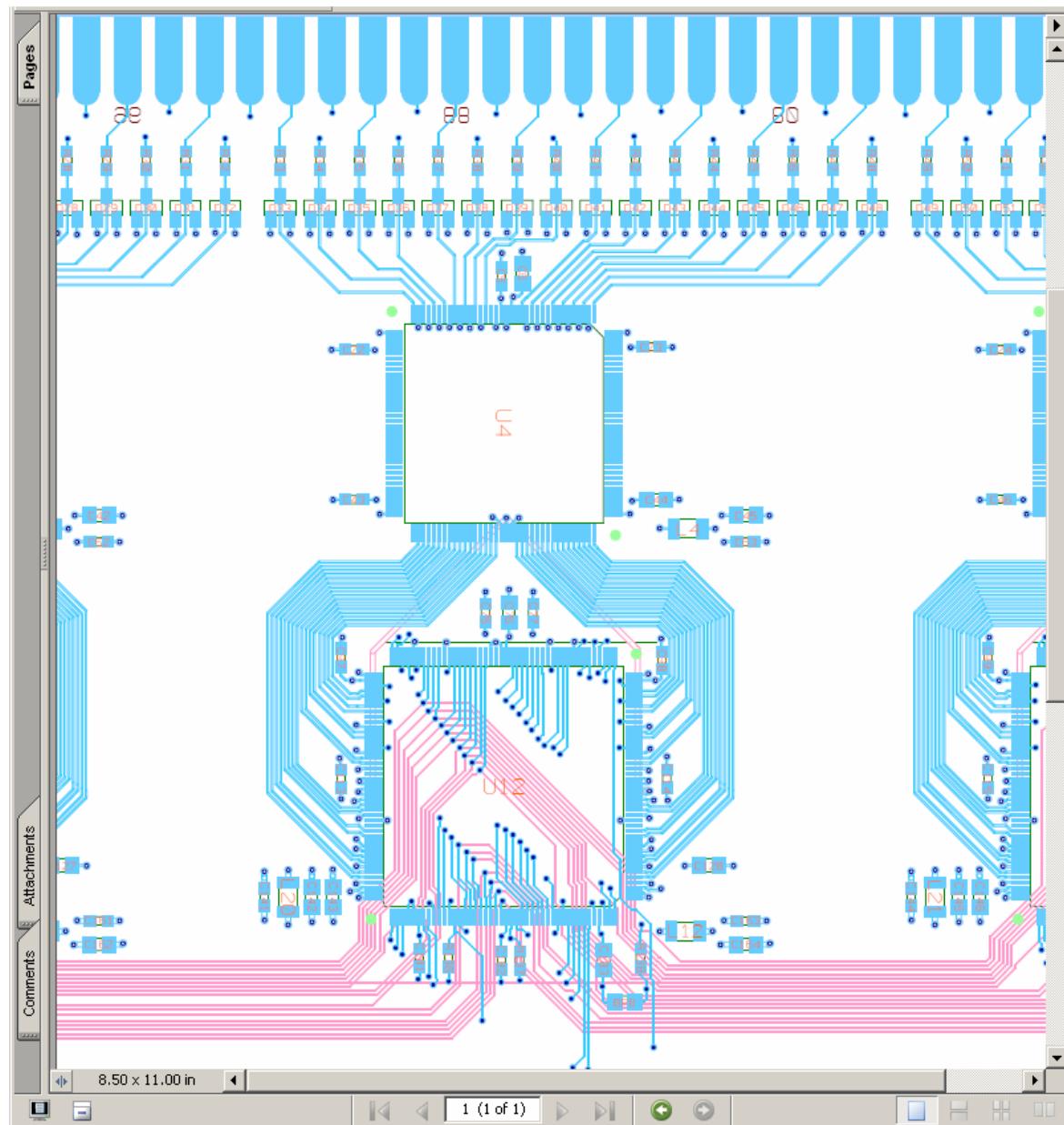
## Layout of Stick with Pasa/Altro chip set



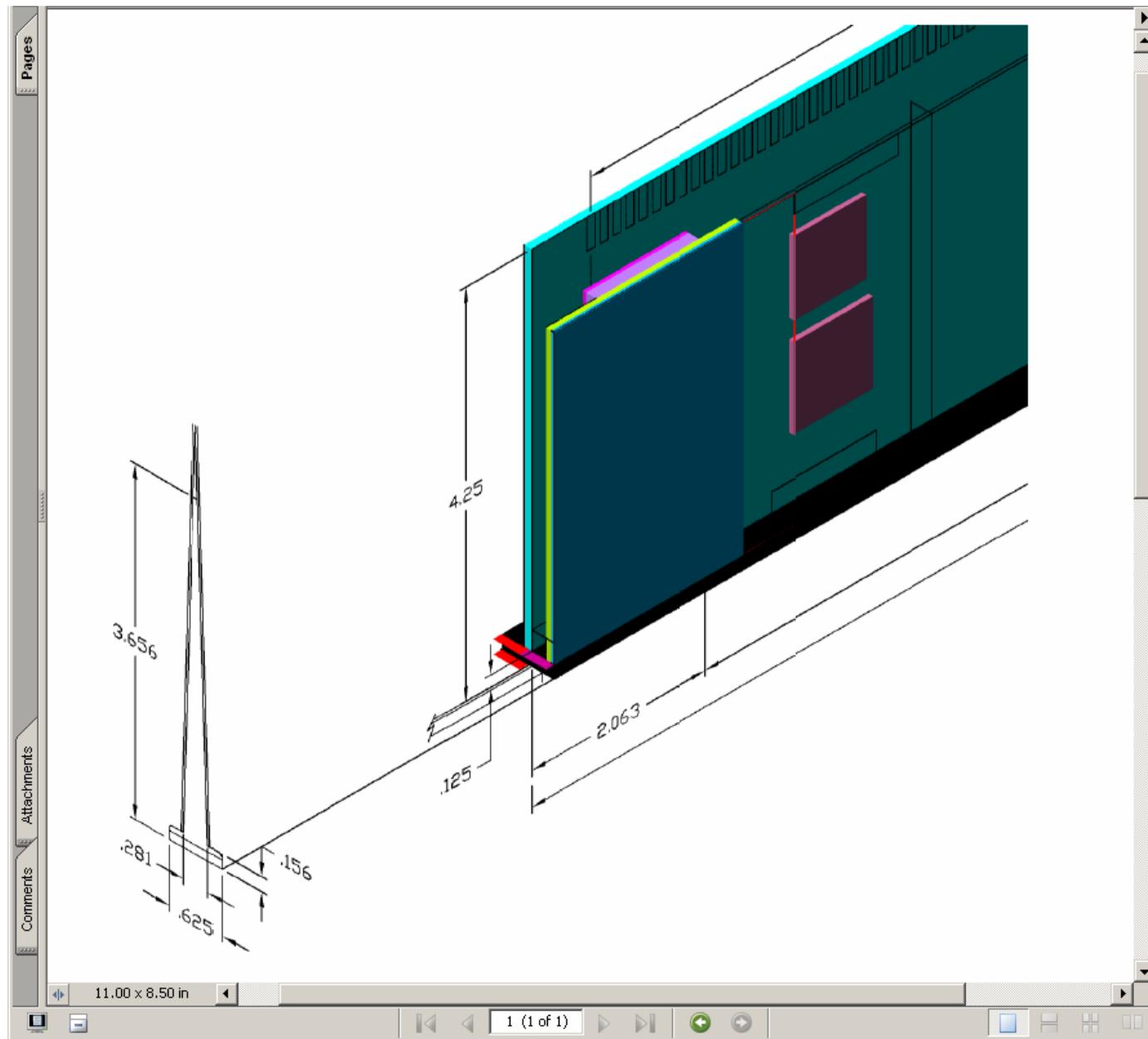
# Closeup of T connection Layout of Stick with Pasa/Altro chip set



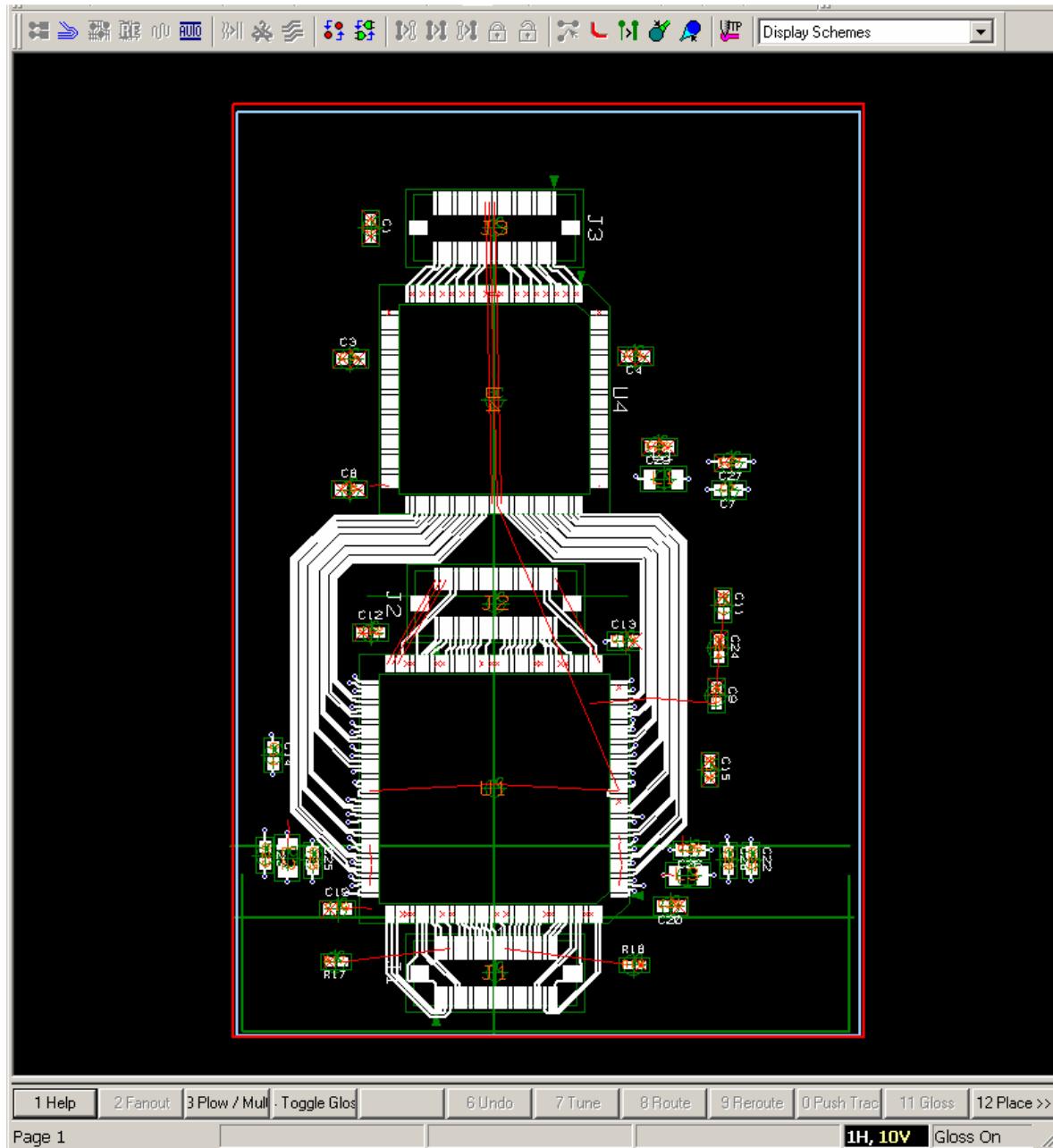
# Close up of small stub connection Layout of Stick with Pasa/Altro chip set



# Mechanical view of design using a daughter card for Pasa/Altro chip set



# Layout of Stick with daughter card for Pasa/Altro chip set



**Adobe Reader - [103780.pdf]**

File Edit View Document Tools Window Help

106%

**Metro Circuits**  
Division of PJC Technologies, Inc.  
205 LaGrange Avenue Rochester NY 14613  
Tel: 585-254-2980 Fax: 585-254-4614  
email: sales@metrocircuits.com

**Quoted To:**  
FERMI LABS

**Quotation**

Quotation Number: **103780**  
Date: **9/20/2006**  
Good Through: **10/20/2006**

Payment Terms:  
Ship Via:  
F.O.B: **Origin**  
Sales Person: **JB**

**Attention:** NINA MOIBENKO      **Fax:**

---

<b>Part Number</b>	<b>Rev</b>	<b>Delivery</b>	<b>Quantity</b>	<b>Price Each</b>	<b>Extension</b>
FEC PASA ALTO CON		10 DAYS	3	\$1,125.00	\$3,375.00
		20 DAYS	120	\$180.00	\$21,600.00

**Non-Recurring and Test Charges:**

**PWB Specification:**

General Information	Finishes	Technology
Material Type : FR4		
Layer Count : 10		
Board Size : 4.25 x 20.63	Soldermask Color : GREEN	
	Soldermask Sides : 2 SIDES	
Finished Thickness : .063	Legend Sides : 2 SIDES	

**Special Requirements/Comments**

SET UP/TEST CHARGES WAIVED 3 BOARDS - MIN LOT SIZE  
DUAL NI/AU FINISH (FLASH ENTIRE BOARD/HARD AU @ CONNECTOR)  
INSTEAD OF SPECIFIED TIN/HARD AU

**Terms & Conditions:**

Price and delivery subject to receipt and verification of gerber files, drill files and fabrication drawings. Any changes after quotation may require a revised quotation.

All deliveries are quoted in working days, excluding weekends and legal holidays. Delivery time quoted as "shipping X days ARO (after receipt of order) or ARM (after receipt of materials)."

Delivery based on availability of material upon receipt of purchase order.

Quotation is valid for 30 days.

No returns after 30 days or after further processing. Metro Circuits' liability is limited to replacement of bare boards only.

Credit terms are subject to credit check and approval. We accept VISA, Mastercard and AMEX.

Unless otherwise specified by customer, manufacturing to be in accordance with IPC-A-6012, Class II for rigid boards or IPC-A-6013 Class II for flex boards.

**Adobe Reader - [104398.pdf]**

File Edit View Document Tools Window Help

Pages Attachments Comments

**Metro Circuits**  
Division of PJC Technologies, Inc.  
205 LaGrange Avenue Rochester NY 14613  
Tel: 585-254-2980 Fax: 585-254-4614  
email: sales@metrocircuits.com

**Quoted To:**  
FERMI LABS

**Quotation**

Quotation Number: **104398**  
Date: **11/16/2006**  
Good Through: **12/16/2006**

Payment Terms:  
Ship Via:  
F.O.B: **Origin**  
Sales Person: **JB**

**Attention:** NINA MOIBENKO      **Fax:**

---

<b>Part Number</b>	<b>Rev</b>	<b>Delivery</b>	<b>Quantity</b>	<b>Price Each</b>	<b>Extension</b>
FEC PASA ALTRO MOTHER		10 DAYS	3	\$820.00	\$2,460.00
		30 DAYS	130	\$160.00	\$20,800.00

**Non-Recurring and Test Charges:**

**PWB Specification:**

General Information	Finishes	Technology
Material Type : FR4	Surface Finish : IMMERSION TIN	
Layer Count : 4	Soldermask Color : GREEN	
Board Size : 4.25 x 20.63	Soldermask Sides : 2 SIDES	
Finished Thickness : 0.063	Legend Sides : 2 SIDES	

**Special Requirements/Comments**  
3 BOARDS - MINIMUM LOT SIZE (1 PANEL)  
SET UP/TEST CHARGES WAIVED

**Terms & Conditions:**

Price and delivery subject to receipt and verification of gerber files, drill files and fabrication drawings. Any changes after quotation may require a revised quotation.

All deliveries are quoted in working days, excluding weekends and legal holidays. Delivery time quoted as "shipping X days ARO (after receipt of order) or ARM (after receipt of materials)."

Delivery based on availability of material upon receipt of purchase order.

Quotation is valid for 30 days.

No returns after 30 days or after further processing. Metro Circuits' liability is limited to replacement of bare boards only.

Credit terms are subject to credit check and approval. We accept VISA, Mastercard and AMEX.

Unless otherwise specified by customer, manufacturing to be in accordance with IPC-A-6012, Class II for rigid boards or IPC-A-6013 Class II for flex boards.

We are an ISO 9001:2000 and AS9100:2004 certified company.

1 of 1

**Adobe Reader - [104399.pdf]**

File Edit View Document Tools Window Help

Pages Attachments Comments

**Metro Circuits**  
Division of PJC Technologies, Inc.  
205 LaGrange Avenue Rochester NY 14613  
Tel: 585-254-2980 Fax: 585-254-4614  
email: sales@metrocircuits.com

**Quoted To:**  
FERMI LABS

**Quotation**

Quotation Number: **104399**  
Date: **11/16/2006**  
Good Through: **12/16/2006**

Payment Terms:  
Ship Via:  
F.O.B: **Origin**  
Sales Person: **JB**

**Attention:** NINA MOIBENKO      **Fax:**

---

<b>Part Number</b>	<b>Rev</b>	<b>Delivery</b>	<b>Quantity</b>	<b>Price Each</b>	<b>Extension</b>
FEC PASA ALTRO DOTER		10 DAYS	16	\$120.00	\$1,920.00
		30 DAYS	1040	\$16.50	\$17,160.00

**Non-Recurring and Test Charges:**

**PWB Specification:**

General Information	Finishes	Technology
Material Type : FR4	Surface Finish : IMMERSION TIN	
Layer Count : 10	Soldermask Color : GREEN	
Board Size : 2.56 x 3.71	Soldermask Sides : 2 SIDES	
Finished Thickness : 0.063	Legend Sides : 2 SIDES	

**Special Requirements/Comments**  
SET UP/TEST CHARGES WAIVED

**Terms & Conditions:**

Price and delivery subject to receipt and verification of gerber files, drill files and fabrication drawings. Any changes after quotation may require a revised quotation.

All deliveries are quoted in working days, excluding weekends and legal holidays. Delivery time quoted as "shipping X days ARO (after receipt of order) or ARM (after receipt of materials)."

Delivery based on availability of material upon receipt of purchase order.

Quotation is valid for 30 days.

No returns after 30 days or after further processing. Metro Circuits' liability is limited to replacement of bare boards only.

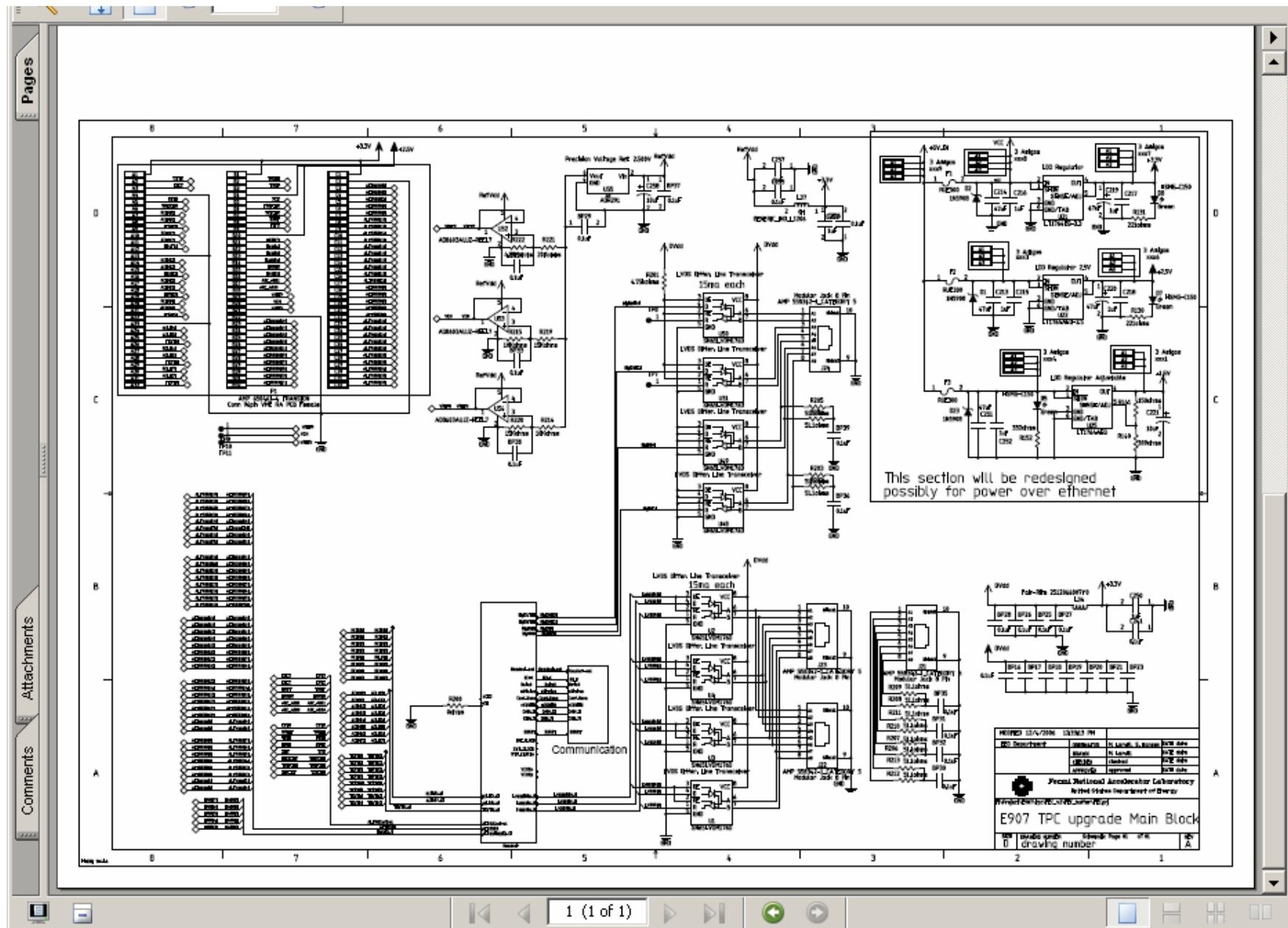
Credit terms are subject to credit check and approval. We accept VISA, Mastercard and AMEX.

Unless otherwise specified by customer, manufacturing to be in accordance with IPC-A-6012, Class II for rigid boards or IPC-A-6013 Class II for flex boards.

We are an ISO 9001:2000 and AS9100:2004 certified company.

1 of 1

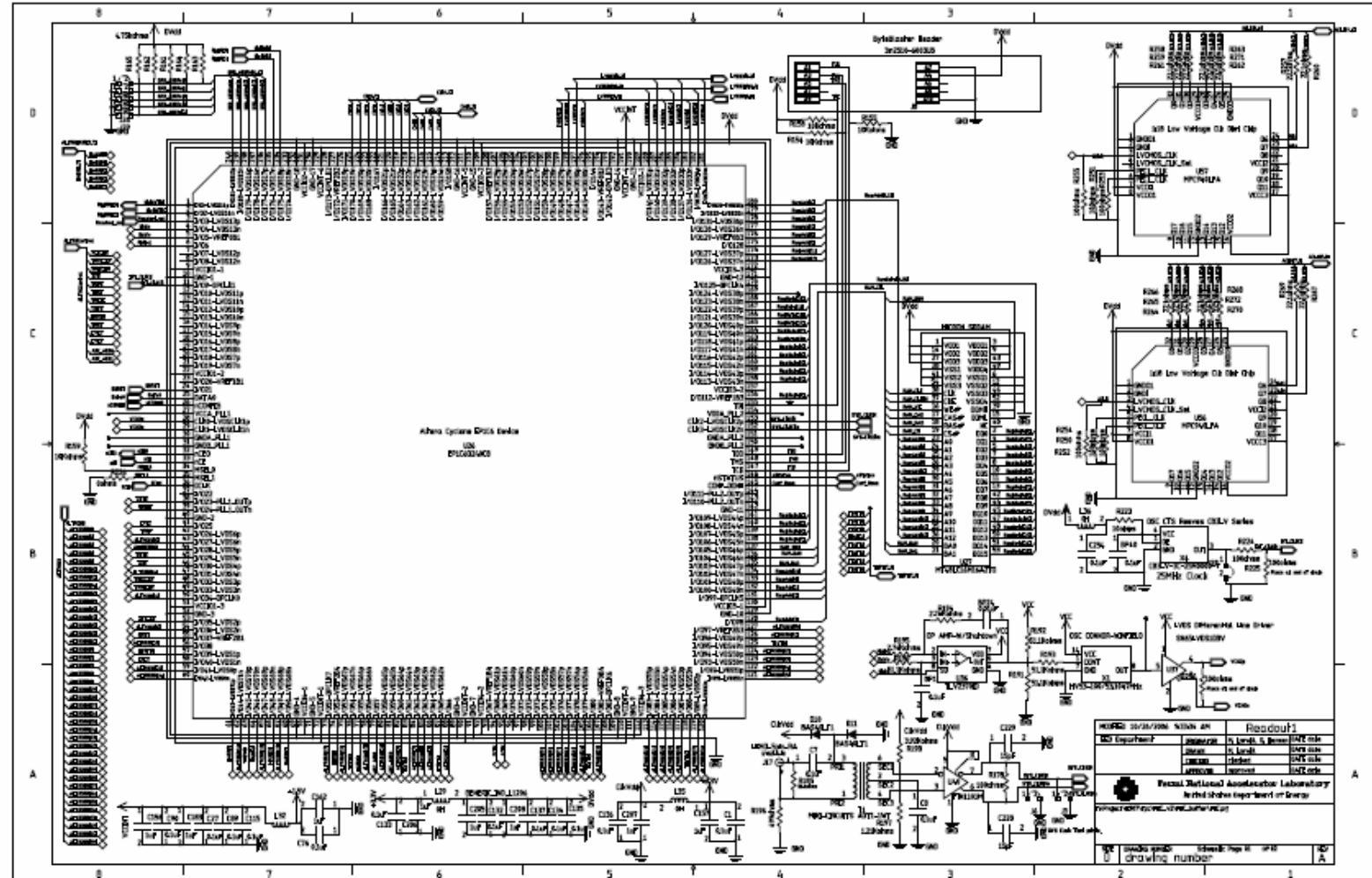
# Schematic of Stick Readout logic for Pasa/Altro chip set



# Adobe Reader - [Readout.sbk(Main.pdf)]

File Edit View Document Tools Window Help

82%



# Adobe Reader - [Communication.sbk(Main.pdf)]

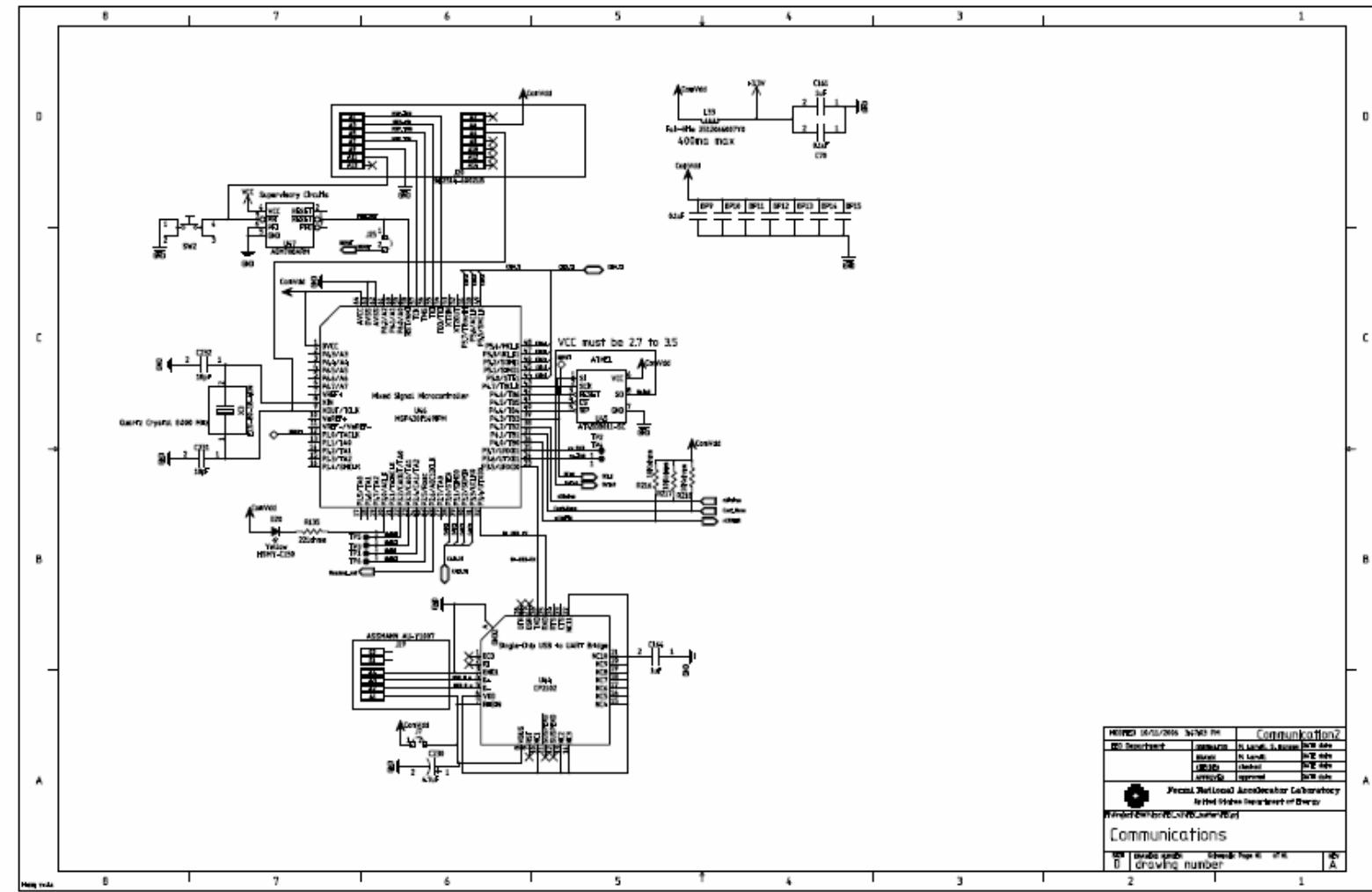
File Edit View Document Tools Window Help

82%

Pages

Attachments

Comments

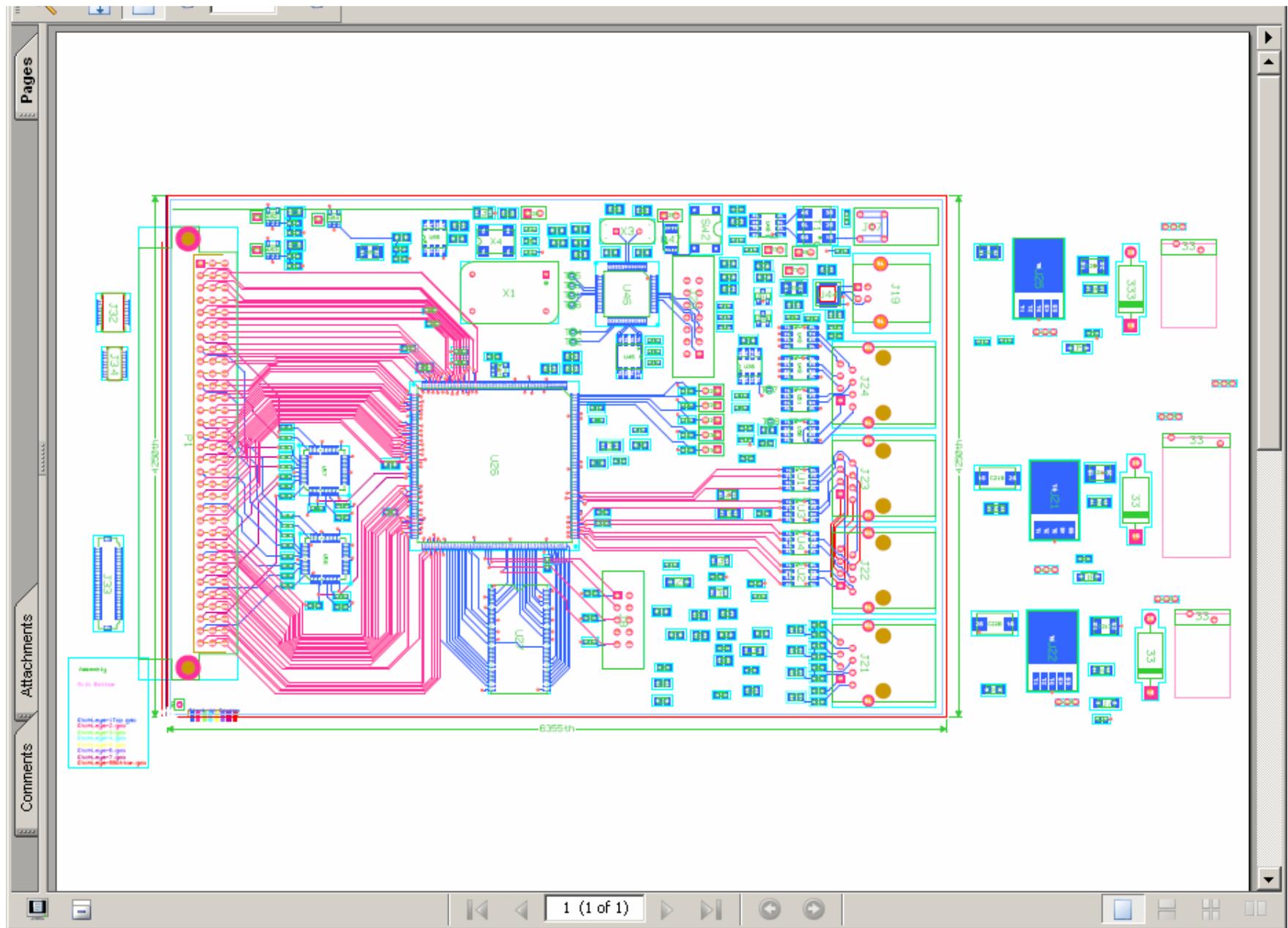


REF ID: 3675/2004 34793 PH	Communication?
PCB designer:	H. Lund, S. Rasmussen
Review:	H. Lund
Approved:	H. Lund
Date:	08/04/2004
Comments:	Not yet reviewed
Project:	Project Name: 34793
Design Center:	Design Center: 34793
Comments:	None
Print date:	08/04/2004
Drawing number:	A

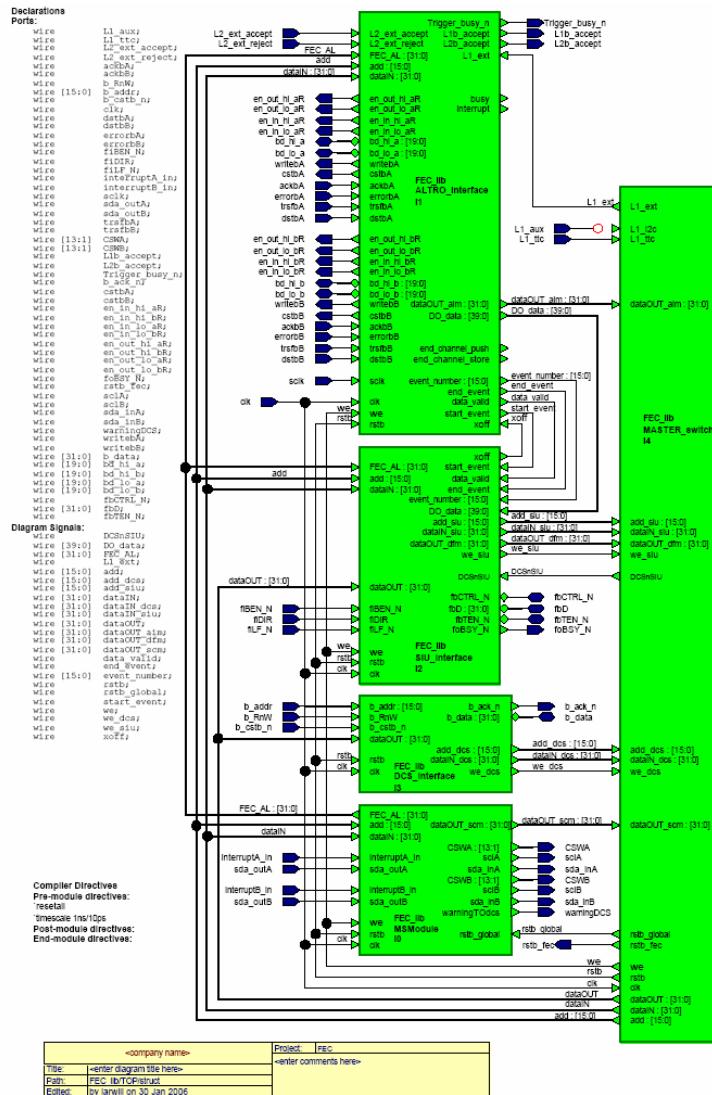


◀ ▶ 1 (1 of 1) ▶ ▶

# Layout of Stick Readout logic for Pasa/Altro chip set



# Block diagram of FPGA code for Readout logic of Pasa/Altro chip set



## Alice readout card power should be similar to ours

Pages

Attachments

Comments

4.6 EPCI441

The configuration EEPROM for the FPGA, which implements the board controller, is supplied at 3.3V. This device together with the monitoring ADC has a power consumption of 4mW.

4.7 FEC total power consumption

For the calculation of the total power consumption the voltage drop across the regulators and the main switch has to be considered:

- Volt. Regulator for the 3.3 V:  $V_{IN} - V_{OUT} = 450\text{mV}$
- Volt. Regulator for the 2.5V:  $V_{IN} - V_{OUT} = 500\text{mV}$
- Main Switch:  $V_{IN} - V_{OUT} = 100\text{mV}$

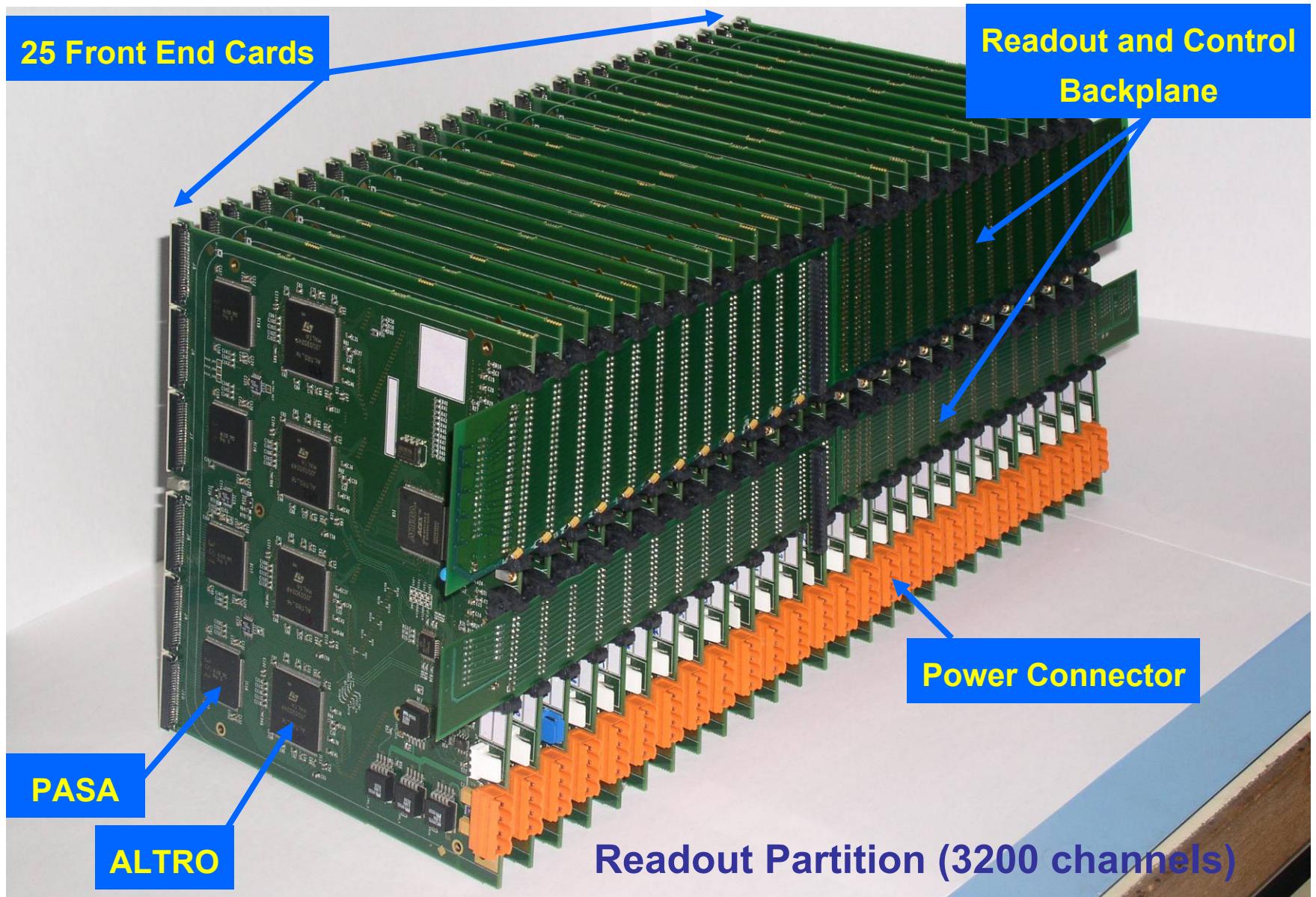
The overall FEC power consumption is summarized in tab.6, which lists the average and peak values for the currents and power, for the two supply voltages, and the total power consumption.

VOLTAGES		AVERAGE		PEAK	
		current (A)	power (W)	current (A)	power (W)
2.5 V		1.1	3.6	1.6	5.3
3.3 V		0.47	1.9	0.47	1.9
Total		1.6	<b>5.5</b>	2.1	<b>7.2</b>

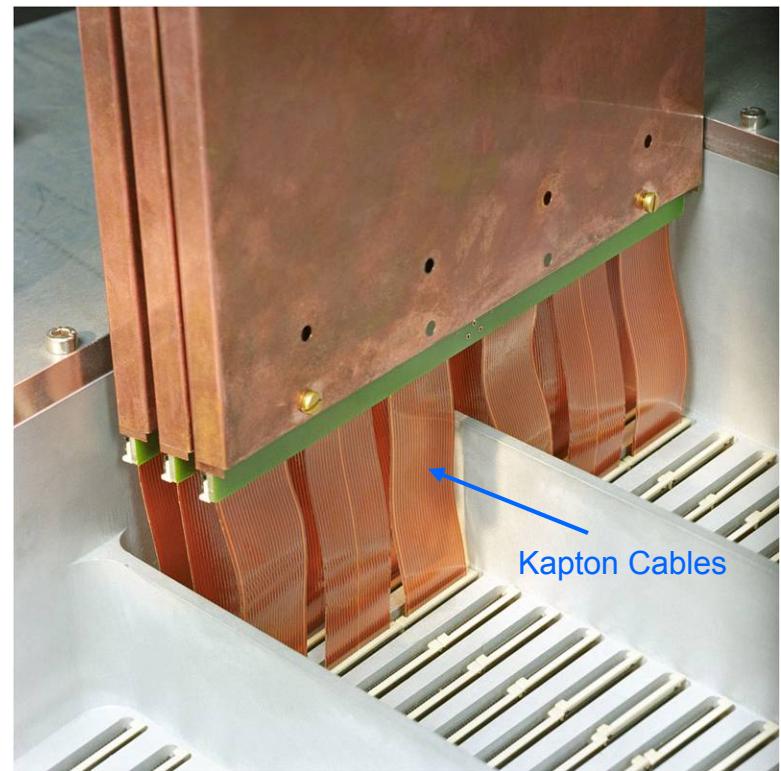
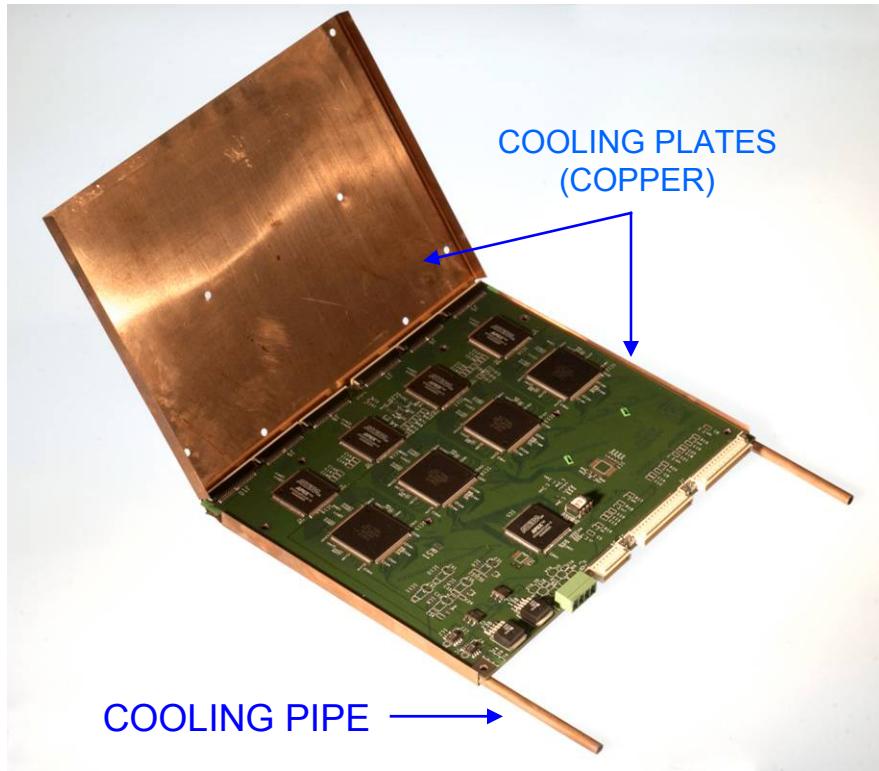
Tab. 6. Average and peak values for the current and power of the FEC

12 of 30

Alice readout cards mechanical arrangement



## Readout card cooling



- Production of 4500 copper plates in progress. Half have been produced
- Delivery: 1<sup>st</sup> lot Dec 04, 2<sup>nd</sup> lot Mar 05

Milestone #230, FEE cables

- Production of 30K kapton cables completed
- Full delivery end Nov 04



## Radiation Tolerance Strategy

- Decide to migrate RCU-FPGA to XILINX
  - SEU per Run (4 hours) = 3.7 => Not acceptable without reconfiguration
  - ALTERA FPGAs do not provide real-time readback of configuration data
  - Partial configuration while running upon error detection
- Decide to keep DCS board unchanged
- Port RCU design to new development environment
- Redundancy / triple voting schemes for vital circuits
- Verify expected performance under irradiation
  - XILINX test @ OCL in August '04
  - System test @ TSL Q1 205 with large beam spot in May '05