

New Electronics for MIPP Plastic Ball

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December 9, 2006

Initial Requirements So Far..

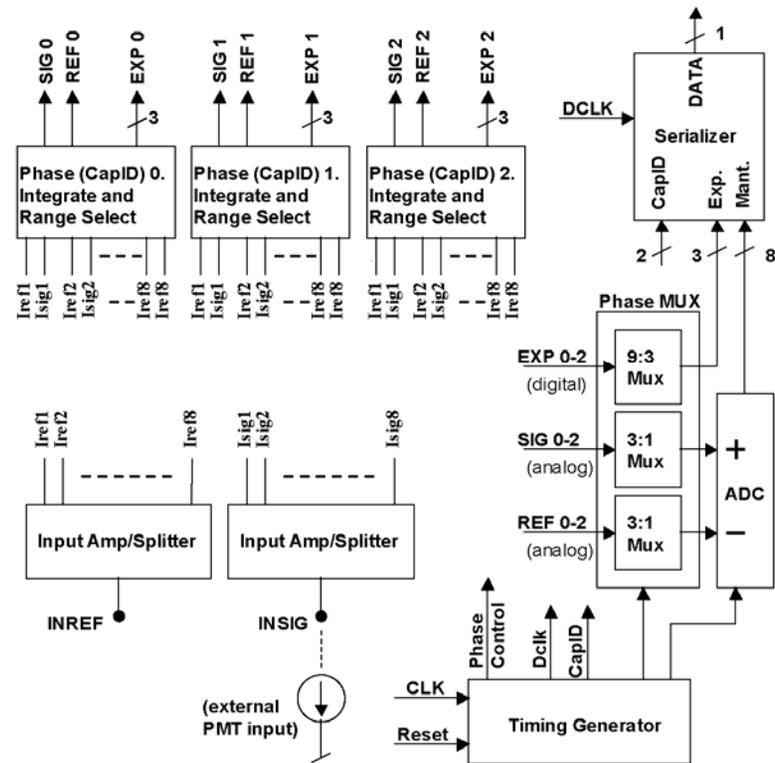
- Charge measurements with separation of fast (~ 10 ns) and slow (~ 1 μ S) PMT signal components
- Multi-hit time measurements with a fraction of a nanosecond resolution
- Trigger capability (maybe not needed)??
- Trigger rates of several kHz (≤ 3 kHz)

BTeV QIE9 integrating ADC (1)

- Developed by Tom Zimmerman FNAL/EED ^[1]
- 8 bit resolution ($<0.24\%$), 16 bit dynamic range
- Uses 8 binary weighted QIE ranges, 8 bit ADC
- Calibration required: slope and offset constants per range, possibly per phase
- LSB = 5 fC, maximum charge = 320 pC
- Noise < 1 LSB
- QIE clock period is 132 ns (possibly 100 ns)
- 14 bit serial output: 8 bit mantissa, 3 bit exponent, 2 bit CapID code, 1 spare. Readout clock period 9.4 ns sync'd with 132 ns QIE clock

BTeV QIE9 integrating ADC (2)

- Adjustable 50 ohm input impedance
- PMT anode floats at QIE input offset voltage (≥ 1 Mohm load resistor)
- Input peak current ≤ 20 mA
- Intrinsic pipeline delay of three clock cycles allows deadtimeless operations



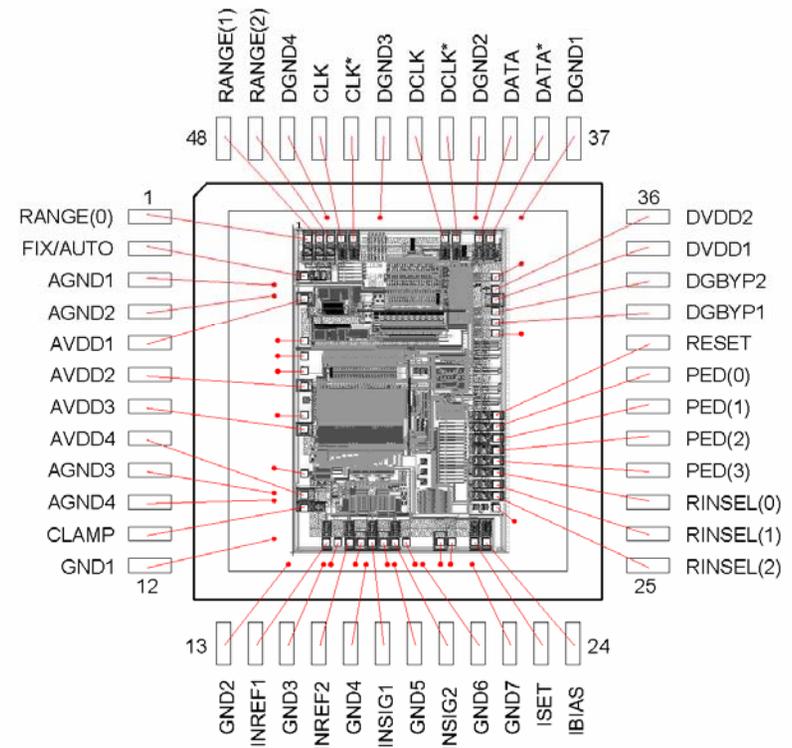
Block-diagram of the QIE9 chip

BTeV QIE9 integrating ADC (3)

- 195 packaged *untested* QIE9 chips are on hand
- 200 *additional* diced chips are available at €62 a piece
- With estimated yield ~80% this may produce total of ~320 working chips
- Additional few thousands of chips are available through 2008 via dedicated run for €59,800 (min. 2 wafers, up to 4 additional wafers €2,900 each)

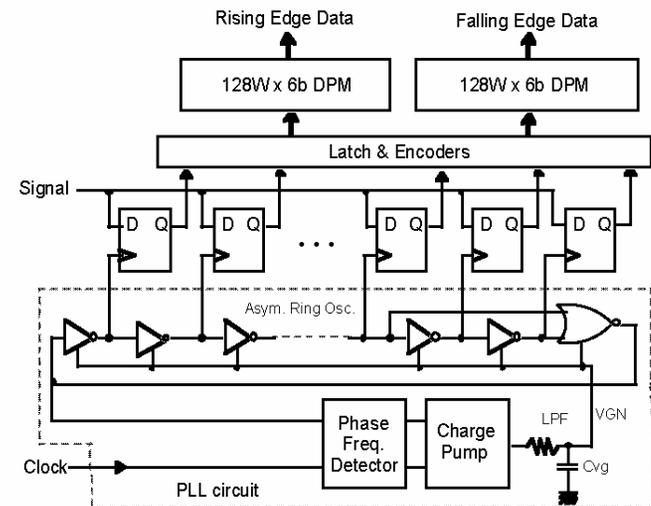
QIE 9 Prototype Pinout
48-Lead TQFP Package Bonding Diagram

(Drawing **NOT** to Scale)



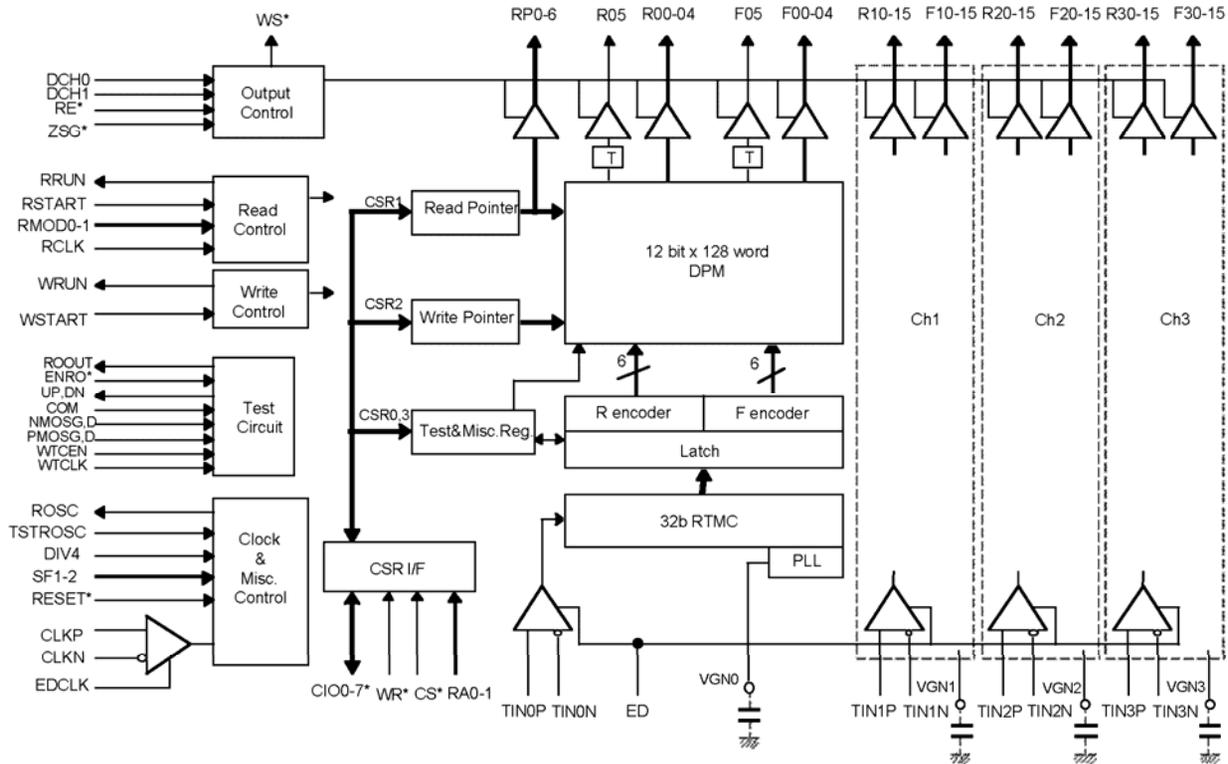
D0 TMC304 Time Digitizer (1)

- Developed by Yasuo Arai KEK ^[2]
- Least Time Count : 0.6 -3.1 ns/bit
- Time Resolution : RMS = 250 ps (@40 MHz)
- Integral Linearity Error : < 80 ps @40MHz
- Differential Linearity Error : < 60 ps @40MHz
- System Clock Frequency : 10 - 50 MHz (x1 mode, 53.1 MHz possible)
- No. of Channels : 4 Channels
- Recording depth : 128 clock cycles (2.56 -12.8 μ s)
- Double Hit Resolution : 25 - 32 ns
- Deadtimeless operations ^[3]



TMC time digitizer logic

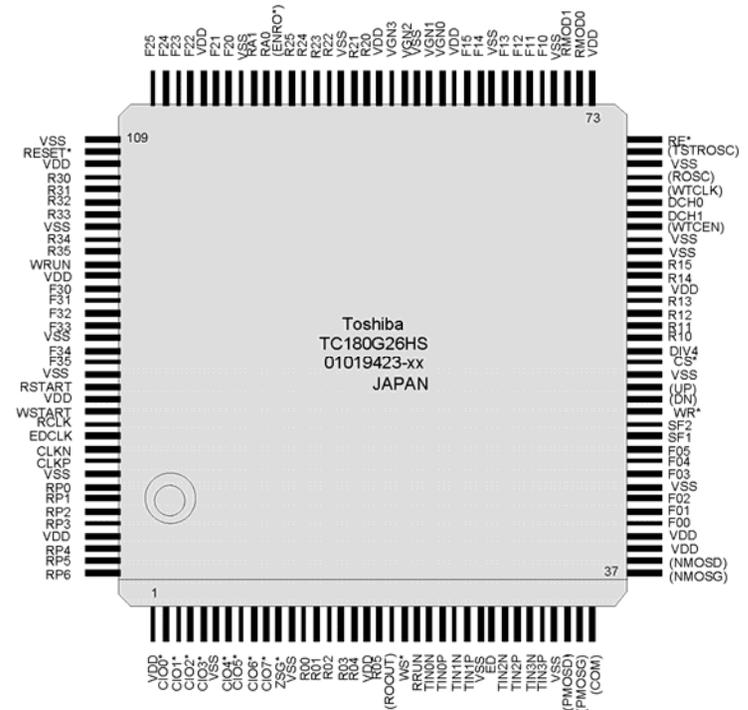
D0 TMC304 Time Digitizer (2)



TMC304 Block Diagram

D0 TMC304 Time Digitizer (3)

- D0 experiment has about 400 TMC304 spare chips (MIPP needs ~100 ea)
- Only a few out of 1872 chips were replaced during five years of operations



TMC304 chip

Current Status and Plans

- Work on QIE9 test fixture just started
- Need to discuss and prepare Plastic Ball Front-End (PBFEE) design specification soon
- If PBFEE design is approved, first prototype may be available in 4..6 months
- Specification of the Readout Interface has to be complete and be available soon

References

- [1] T.Zimmerman, QIE9 Technical Manual, Fermilab, v1.0, July 28, 2004, Unpublished.
- [2] Y.Arai, TMC304(TEG3) User's manual, KEK, v1.4, November 13, 1996, Unpublished
- [3] B.Baldin, et al. "D0 Muon Readout Electronics Design," IEEE Trans. on Nuclear Science, Vol.44, No.3, pp 363-369, June 1997